Miscellaneous Design Tips and Facts

Introduction

This application note presents design tips and facts on the following topics:

- Relationship of I_{AV}, I_{RMS}, and I_{PK}
- dv/dt Definitions
- Examples of gate terminations
- Curves for Average Current at Various Conduction Angles
- Double-exponential Impulse Waveform
- Failure Modes of Thyristor
- Characteristics Formulas for Phase Control Circuits

Relationship of I_{AV}, I_{RMS}, and I_{PK}

Since a single rectifier or SCR passes current in one direction only, it conducts for only half of each cycle of an AC sinewave. The average current (I_{AV}) then becomes half of the value determined for full-cycle conduction, and the RMS current (I_{RMS}) is equal to the square root of half the mean-square value for full-cycle conduction or half the peak current (I_{PK}). In terms of half-cycle sinewave conduction (as in a single-phase half-wave circuit), the relationships of the rectifier currents can be shown as follows:

$I_{PK} = \pi \bullet I_{AV} = 3.14 \bullet I_{AV}$

$I_{AV} = (1/\pi)\ I_{PK} = 0.32 \bullet I_{PK}$

$I_{PK} = 2 \bullet I_{RMS}$

$I_{RMS} = 0.5 \bullet I_{PK}$

$I_{AV} = (2/\pi)\ I_{RMS} = 0.64 \bullet I_{RMS}$

$I_{RMS} = (\pi/2)\ I_{AV} = 1.57 \bullet I_{AV}$

When two identically rated SCRs are connected inverse parallel for full-wave operation, as shown in Figure AN1009.1, they can handle 1.41 times the RMS current rating of either single SCR. Therefore, the RMS value of two half sinewave current pulses in one cycle is √2 times the RMS value of one such pulse per cycle.

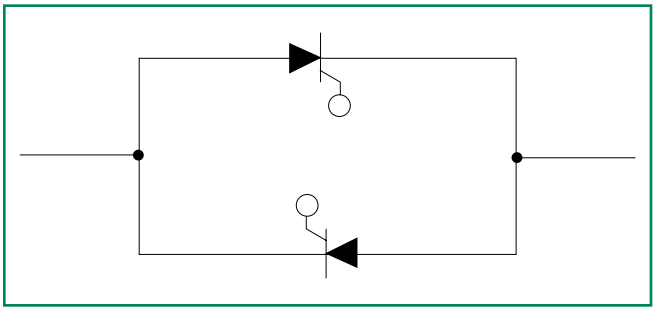


Figure AN1009.1 SCR Anti-parallel Circuit

dv/dt Definitions

The rate-of-rise of voltage (dv/dt) of an exponential waveform is 63% of peak voltage (excluding any overshoots) divided by the time at 63% minus 10% peak voltage. (Figure AN1009.2)

Exponential dv/dt = $0.63 \bullet [V_{PK}] = (t_2 - t_1)$

Resistor Capacitor circuit t = RC = $(t_2 - t_1)$

Resistor Capacitor circuit $4 \bullet RC = (t_3 - t_2)$

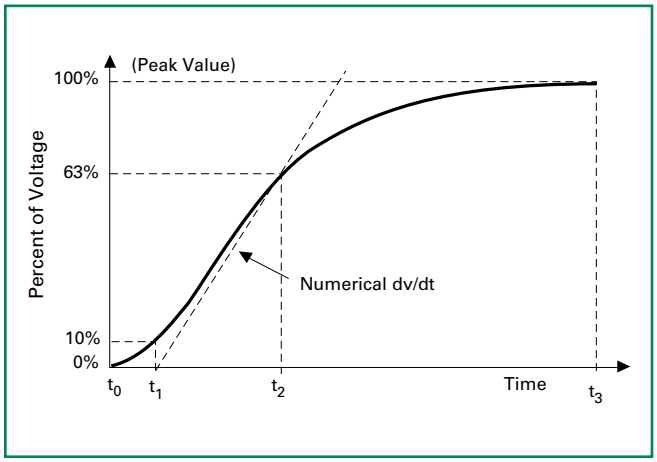


Figure AN1009.2 Exponential dv/dt Waveform

The rate-of-rise of voltage (dv/dt) of a linear waveform is 80% of peak voltage (excluding any overshoots) divided by the time at 90% minus 10% peak voltage. (Figure AN1009.3)

Linear dv/dt = $0.8 = [V_{PK}] = (t_2 - t_1)$

Linear dv/dt = $[0.9 \bullet V_{PK} - 0.1 \bullet V_{PK}] = (t_2 - t_1)$

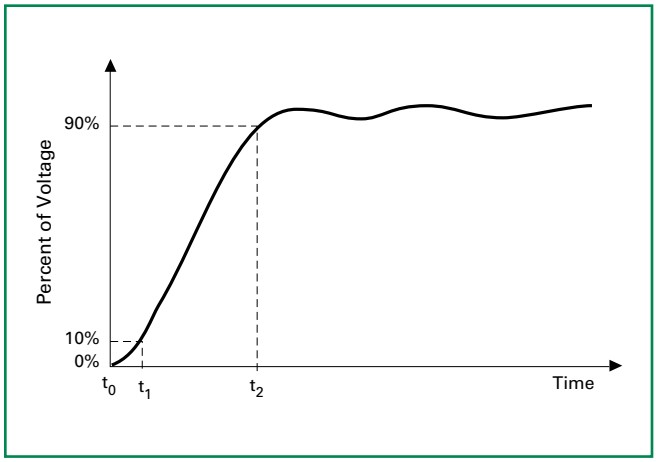
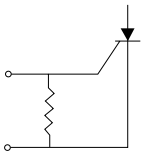


Figure AN1009.3 Linear dv/dt Waveform

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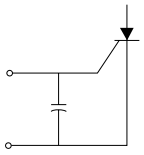
Examples of Gate Terminations



Primary Purpose

(1) Increase dv/dt capability
(2) Keep gate clamped to ensure V_{DRM} capability
(3) Lower t_q time

Related Effect – Raises the device latching and holding current

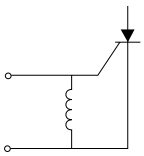


Primary Purpose

(1) Increase dv/dt capability
(2) Remove high frequency noise

Related Effects

(1) Increases delay time
(2) Increases turn-on interval
(3) Lowers gate signal rise time
(4) Lowers di/dt capability
(5) Increases t_q time

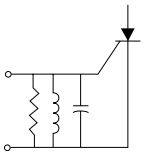


Primary Purpose

(1) Decrease DC gate sensitivity
(2) Decrease t_q time

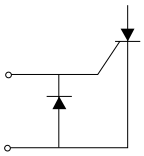
Related Effects

(1) Negative gate current increases holding current and causes gate area to drop out of conduction
(2) In pulse gating gate signal tail may cause device to drop out of conduction



Primary Purpose – Select frequency

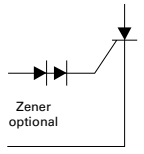
Related Effects – Unless circuit is "damped," positive and negative gate current may inhibit conduction or bring about sporadic anode current



Primary Purpose

(1) Supply reverse bias in off period
(2) Protect gate and gate supply for reverse transients
(3) Lower t_q time

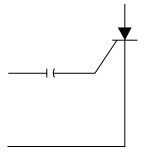
Related Effects – Isolates the gate if high impedance signal source is used without sustained diode current in the negative cycle



Primary Purpose – Decrease threshold sensitivity

Related Effects

(1) Affects gate signal rise time and di/dt rating
(2) Isolates the gate



Primary Purpose – Isolate gate circuit DC component

Related Effects – In narrow gate pulses and low impedance sources, I_{gt} followed by reverse gate signals which may inhibit conduction

Curves for Average Current at Various Conduction Angles

SCR maximum average current curves for various conduction angles can be established using the factors for maximum average current at conduction angle of:

30° = 0.40 x Avg 180°
60° = 0.56 x Avg 180°
90° = 0.70 x Avg 180°
120° = 0.84 x Avg 180°

The reason for different ratings is that the average current for conduction angles less than 180° is derated because of the higher RMS current connected with high peak currents.

Note that maximum allowable case temperature (T_C) remains the same for each conduction angle curve but is established from average current rating at 180° conduction as given in the data sheet for any particular device type. The maximum T_C curve is then derated down to the maximum junction (T_J). The curves illustrated in Figure AN1009.4 are derated to 125 °C since the maximum T_J for the non-sensitive SCR series is 125 °C.

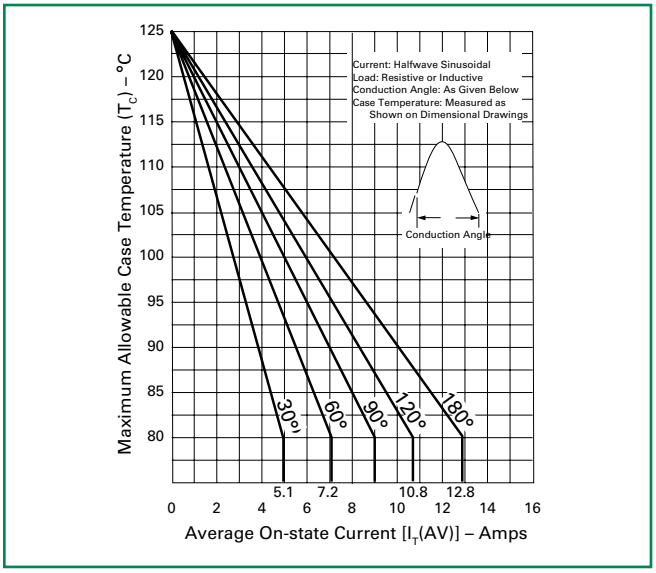


Figure AN1009.4 Typical Curves for Average On-state Current at Various Conduction Angles versus T_C for a SXX20L SCR.

Double-Exponential Impulse Waveform

A double-exponential impulse waveform or waveshape of current or voltage is designated by a combination of two numbers (t_r/t_d or t_r x t_d µs). The first number is an exponential rise time (t_r) or wave front and the second number is an exponential decay time (t_d) or wave tail. The rise time (t_r) is the maximum rise time permitted. The decay time (t_d) is the minimum time permitted. Both the t_r and the t_d are in the same units of time, typically microseconds, designated at the end of the waveform description as defined by ANSI/IEEE C62.1-1989.

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The rise time (t_r) of a current waveform is 1.25 times the time for the current to increase from 10% to 90% of peak value. See Figure AN1009.5.

t_r = Rise Time = 1.25 • [t_c - t_a]

t_r = 1.25 • [t(0.9 I_{PK}) - t(0.1 I_{PK})] = T_1 - T_0

The rise time (t_r) of a voltage waveform is 1.67 times the time for the voltage to increase from 30% to 90% of peak value. (Figure AN1009.5)

t_r = Rise Time = 1.67 • [t_c - t_b]

t_r = 1.67 • [t(0.9 V_{PK}) - t(0.3 V_{PK})] = T_1 - T_0

The decay time (t_d) of a waveform is the time from virtual zero (10% of peak for current or 30% of peak for voltage) to the time at which one-half (50%) of the peak value is reached on the wave tail. (Figure AN1009.5)

Current Waveform t_d = Decay Time

= [t(0.5 I_{PK}) - t(0.1 I_{PK})] = T_2 - T_0

Voltage Waveform t_d = Decay Time

= [t(0.5 V_{PK}) - t(0.3 V_{PK})] = T_2 - T_0

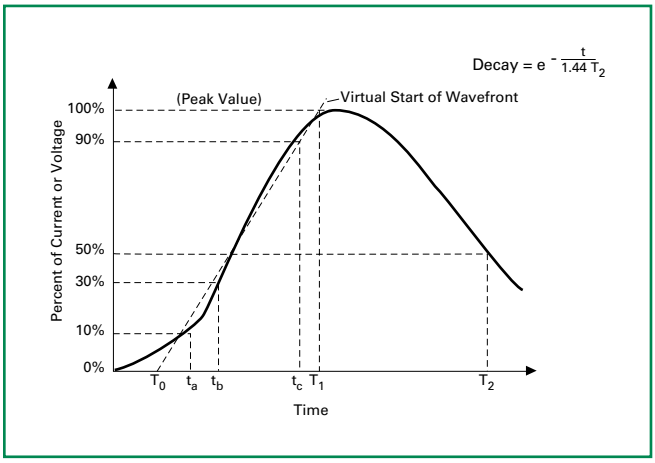


Figure AN1009.5 Double-exponential Impulse Waveform

Failure Modes of Thyristor

Thyristor failures may be broadly classified as either degrading or catastrophic. A degrading type of failure is defined as a change in some characteristic which may or may not cause a catastrophic failure, but could show up as a latent failure. Catastrophic failure is when a device exhibits a sudden change in characteristic that renders it inoperable. To minimize degrading and catastrophic failures, devices must be operated within maximum ratings at all times.

Degradation Failures

A significant change of on-state, gate, or switching characteristics is quite rare. The most vulnerable characteristic is blocking voltage. This type of degradation increases with rising operating voltage and temperature levels.

Catastrophic Failures

A catastrophic failure can occur whenever the Thyristor is operated beyond its published ratings. The most common failure mode is an electrical short between the main terminals, although a Triac can fail in a half-wave condition. It is possible, but not probable, that the resulting short-circuit current could melt the internal parts of the device which could result in an open circuit.

Failure Causes

Most Thyristor failures occur due to exceeding the maximum operating ratings of the device. Overvoltage or overcurrent operations are the most probable cause for failure. Overvoltage failures may be due to excessive voltage transients or may also occur if inadequate cooling allows the operating temperature to rise above the maximum allowable junction temperature. Overcurrent failures are generally caused by improper fusing or circuit protection, surge current from load initiation, load abuse, or load failure. Another common cause of device failure is incorrect handling procedures used in the manufacturing process. Mechanical damage in the form of excessive mounting torque and/or force applied to the terminals or leads can transmit stresses to the internal Thyristor chip and cause cracks in the chip which may not show up until the device is thermally cycled.

Prevention of Failures

Careful selection of the correct device for the application's operating parameters and environment will go a long way toward extending the operating life of the Thyristor. Good design practice should also limit the maximum current through the main terminals to 75% of the device rating. Correct mounting and forming of the leads also help ensure against infant mortality and latent failures. The two best ways to ensure long life of a Thyristor is by proper heat sink methods and correct voltage rating selection for worst case conditions. Overheating, overvoltage, and surge currents are the main killers of semiconductors.

Most Common Thyristor Failure Mode

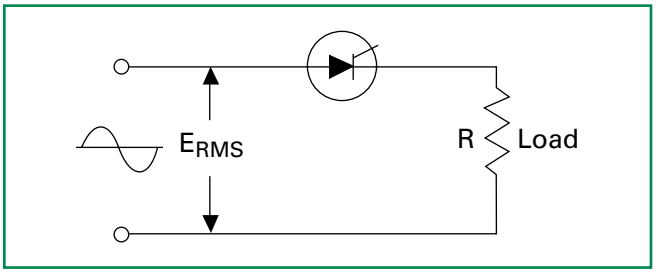
When a Thyristor is electrically or physically abused and fails either by degradation or a catastrophic means, it will short (full-wave or half-wave) as its normal failure mode. Rarely does it fail open circuit. The circuit designer should add line breaks, fuses, over-temperature interrupters or whatever is necessary to protect the end user and property if a shorted or partially shorted Thyristor offers a safety hazard.

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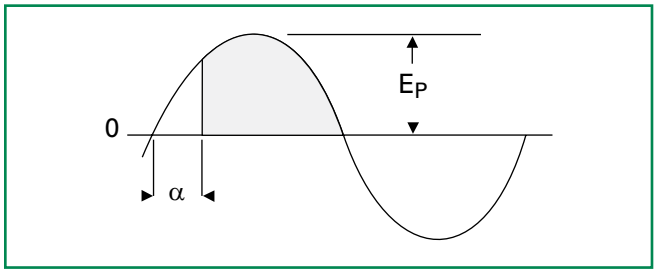
Characteristics Formulas for Phase Control Circuits

Circuit Name	Max Thyristor Voltage	PRV	Max. Load Voltage E_d=Avg. E_a=RMS Load	Load Voltage with Delayed Firing	Max. Average Thyristor or Rectifier Current	
		SCR			Avg. Amps	Conduction Period
Half-wave Resistive Load	1.4 E_{RMS}	E_P	$E_d = \frac{E_p}{\pi}$ $E_a = \frac{E_p}{2}$	$E_d = \frac{E_p}{2\pi}(1+\cos\alpha)$ $E_a = \frac{E_p}{2\sqrt{\pi}}\sqrt{(\pi - \alpha + \frac{1}{2}\sin 2\alpha)}$	$\frac{E_p}{\pi R}$	180°
Full-wave Bridge	1.4 E_{RMS}	E_P	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{2\sqrt{\pi}}(1+\cos\alpha)$	$\frac{E_p}{\pi R}$	180°
Full-wave AC Switch Resistive Load	1.4 E_{RMS}	E_P	$E_a = \frac{E_p}{1.4}$	$E_a = \frac{E_p}{\sqrt{2\pi}}\sqrt{(\pi - \alpha + \frac{1}{2}\sin 2\alpha)}$	$\frac{E_p}{\pi R}$	180°

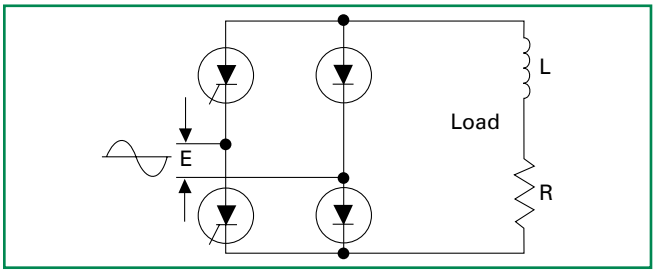
NOTE: Angle alpha (α) is in radians.



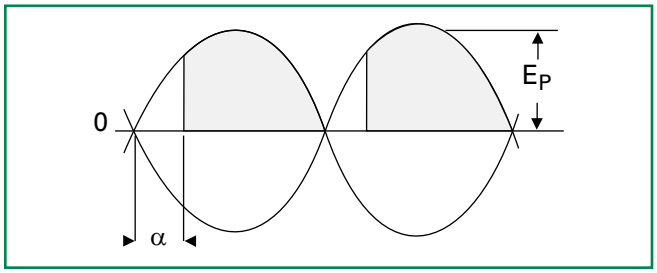
Half-wave Resistive Load - Schematic



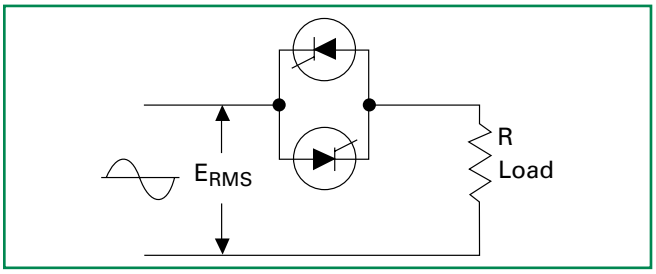
Half-wave Resistive Load - Waveform



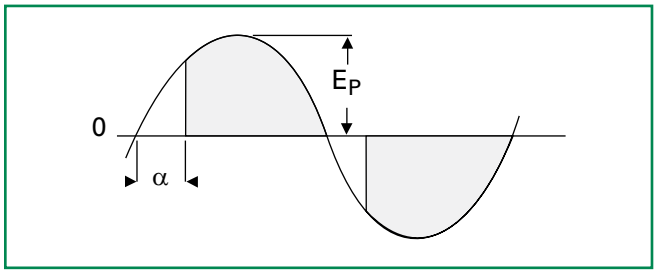
Full-wave Bridge - Schematic



Full-wave Bridge - Waveform



Full-wave AC Switch Resistive Load - Schematic



Full-wave AC Switch Resistive Load - Waveform

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