

Test Report

Fail

Test Configuration Details	
Application	
Name	D9021HDMC HDMI Test
Version	2.33.0.0
Device Description	
HDMITestType	TMDS Physical Layer
DeviceID	Transmitter
Device Name	Device1
Comments	User comments
FixtureType	Wilder HDMI2 TPA-P 12 inch
Probe Head Type	N5444A/N700XA
Probe Connection Choice	4 Probes
Lane Connection	1 Data Lane
Test Session Details	
Infiniium SW Version	06.30.00701
Infiniium Model Number	MSOV204A
Infiniium Serial Number	MY56110101
Debug Mode Used	No
Probe (Channel 1)	Model: N7002A Serial: US55051001 Head: N5444A Atten: Calibrated (1 NOV 2024 11:03:16), Using Cal Atten (1.0101E+01) Skew: Calibrated (1 NOV 2024 11:11:09), Using Cal Skew
Probe (Channel 2)	Model: N7002A Serial: US55051007 Head: N5444A Atten: Calibrated (1 NOV 2024 11:05:18), Using Cal Atten (1.0173E+01) Skew: Calibrated (1 NOV 2024 11:11:51), Using Cal Skew
Probe (Channel 3)	Model: N7002A Serial: US55051052 Head: N5444A Atten: Calibrated (1 NOV 2024 11:07:21), Using Cal Atten (9.7784E+00) Skew: Calibrated (1 NOV 2024 11:12:43), Using Cal Skew
Probe (Channel 4)	Model: N7002A Serial: US55051005 Head: N5444A Atten: Calibrated (1 NOV 2024 11:09:24), Using Cal Atten (1.0002E+01) Skew: Calibrated (1 NOV 2024 11:13:21), Using Cal Skew
Last Test Date	2024-11-05 11:00:51 UTC +08:00

Summary of Results

Test Statistics		Margin Thresholds	
Failed	3	Warning	< 2 %
Passed	29	Critical	< 0 %
Total	32		

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	116 mTbit	53.6	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	210.877 ps	181.2	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	203.085 ps	170.8	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	49.660	24.2	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.290	16.2	<=60%
✓	0	1	7-2: VL Clock +	2.765 V	45.0	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.768 V	44.0	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	6 mTbit	48.0	-150 mTbit <= VALUE <= 150 mTbit
✗	1	1	7-10: D0 Mask Test	266.000	-266E+02	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	163 m	45.7	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	191.527 ps	155.4	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	191.027 ps	154.7	VALUE >= 75.000 ps
✓	0	1	7-2: VL D0+	2.766 V	44.7	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.771 V	43.0	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	-3 mTbit	49.0	-150 mTbit <= VALUE <= 150 mTbit
✗	1	1	7-10: D1 Mask Test	204.000	-204E+02	No Mask Failures
✓	0	1	7-10: D1 Data Jitter	180 m	40.0	<=0.3Tbit
✓	0	1	7-4: D1 Rise Time	170.902 ps	127.9	VALUE >= 75.000 ps
✓	0	1	7-4: D1 Fall Time	167.269 ps	123.0	VALUE >= 75.000 ps
✓	0	1	7-2: VL D1+	2.764 V	45.3	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D1-	2.763 V	45.7	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 1	-8 mTbit	47.3	-150 mTbit <= VALUE <= 150 mTbit
✗	1	1	7-10: D2 Mask Test	4.090000 k	-409E+03	No Mask Failures
✓	0	1	7-10: D2 Data Jitter	197 m	34.3	<=0.3Tbit
✓	0	1	7-4: D2 Rise Time	200.390 ps	167.2	VALUE >= 75.000 ps
✓	0	1	7-4: D2 Fall Time	197.005 ps	162.7	VALUE >= 75.000 ps
✓	0	1	7-2: VL D2+	2.760 V	46.7	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D2-	2.745 V	48.3	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 2	-34 mTbit	38.7	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-6: Inter-Pair Skew - D0/D1	21 mTpixel	44.8	-200 mTpixel <= VALUE <= 200 mTpixel

✔	0	1	7-6: Inter-Pair Skew - D0/D2	-7 mTpixel	48.3	-200 mTpixel <= VALUE <= 200 mTpixel
✔	0	1	7-6: Inter-Pair Skew - D1/D2	-28 mTpixel	43.0	-200 mTpixel <= VALUE <= 200 mTpixel

Report Detail

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✔

7-9: Clock Jitter

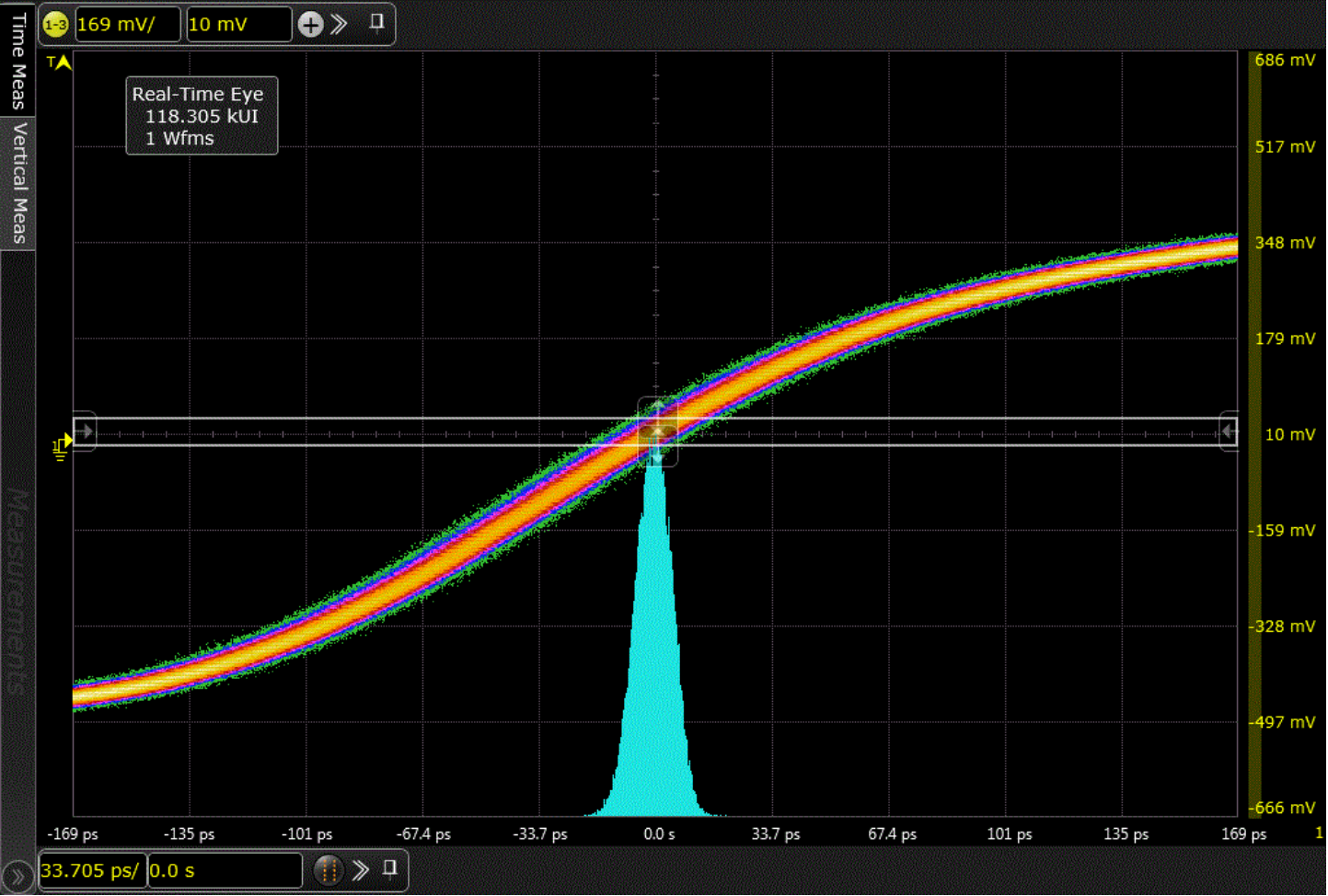
Test ID 7-9

2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.
Actual Value Measurement Name: 7-9 Clock Jitter
Pass Limits: VALUE <= 250 mTbit

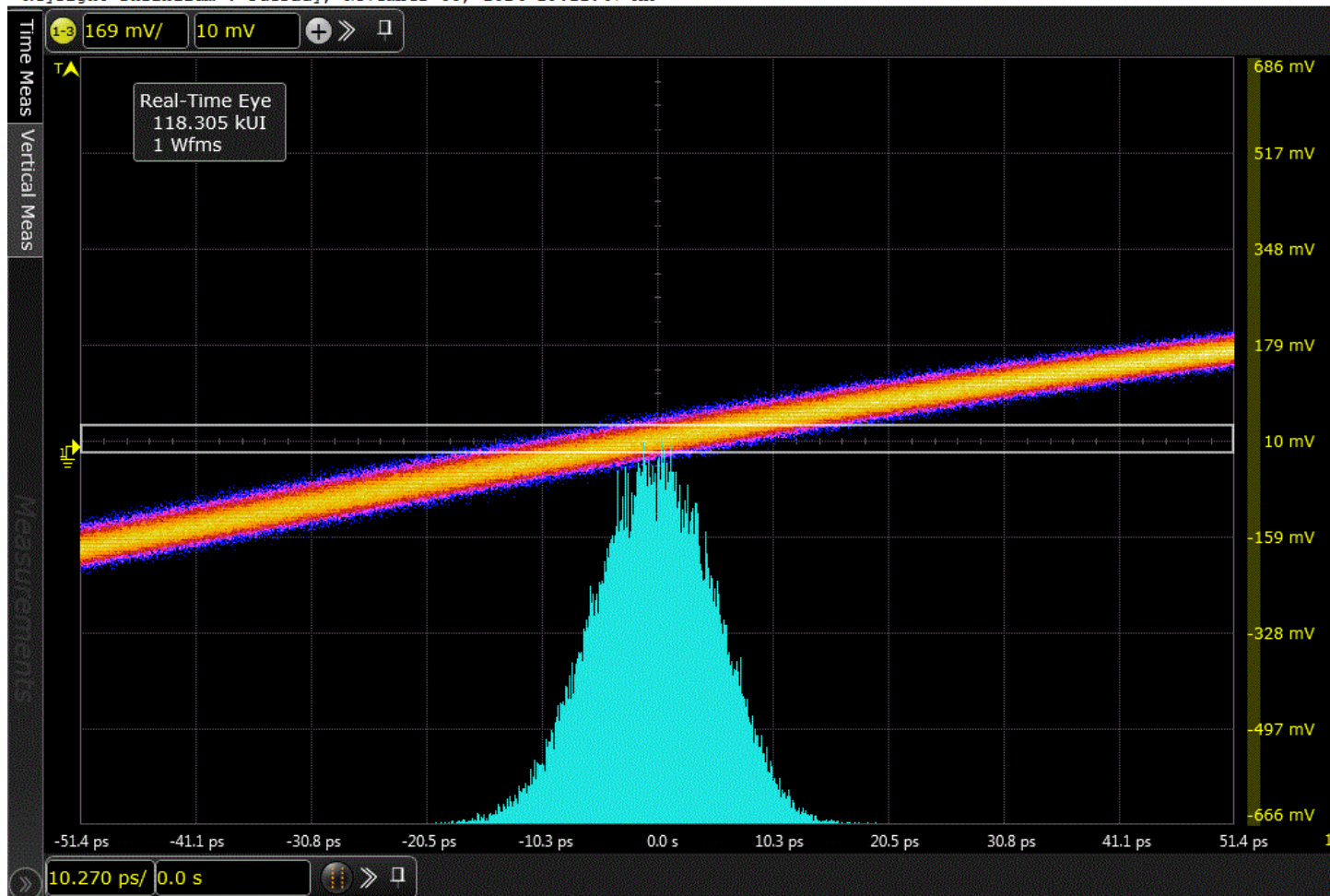
Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Total Jitter with Zoomed Out Screen	Std Dev(ps)	Tbit(ps)
116 mTbit	53.6	Timing 105	296.694 MHz	(See image)	5.253	337.048

Clock Jitter(ps)	# Samples	# Edges	Acquisition Bandwidth (GHz)
39.150	16.000000 M	0	13.000

Total Jitter with Zoomed Out Screen
Keysight Infiniium : Tuesday, November 05, 2024 10:11:30 AM



7-9 Clock Jitter

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Test ID 7-4

2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

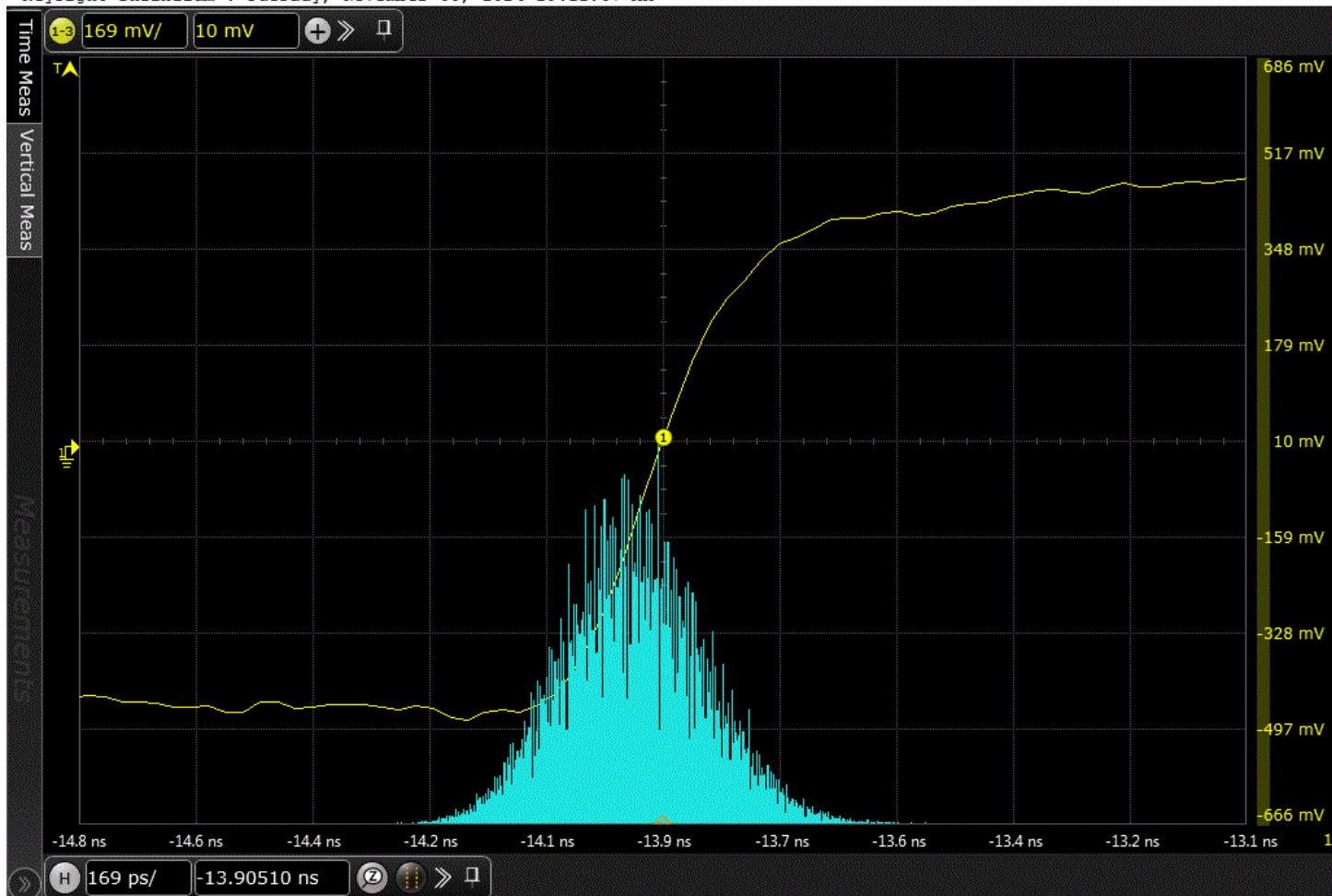
Actual Value Measurement Name: 7-4 Clock Rise Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Upper Threshold(%)	Lower Threshold(%)	VTop(V)	VBase(V)
210.877 ps	181.2	Timing 105	296.694 MHz	80.000	20.000	495 m	-467 m

Upper Threshold(V)	Lower Threshold(V)	# Edges	Acquisition Bandwidth (GHz)
303 m	-275 m	118.677 k	13.000

7-4 Clock Rise Time

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7-4: Clock Fall Time

Test ID 7-4

2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

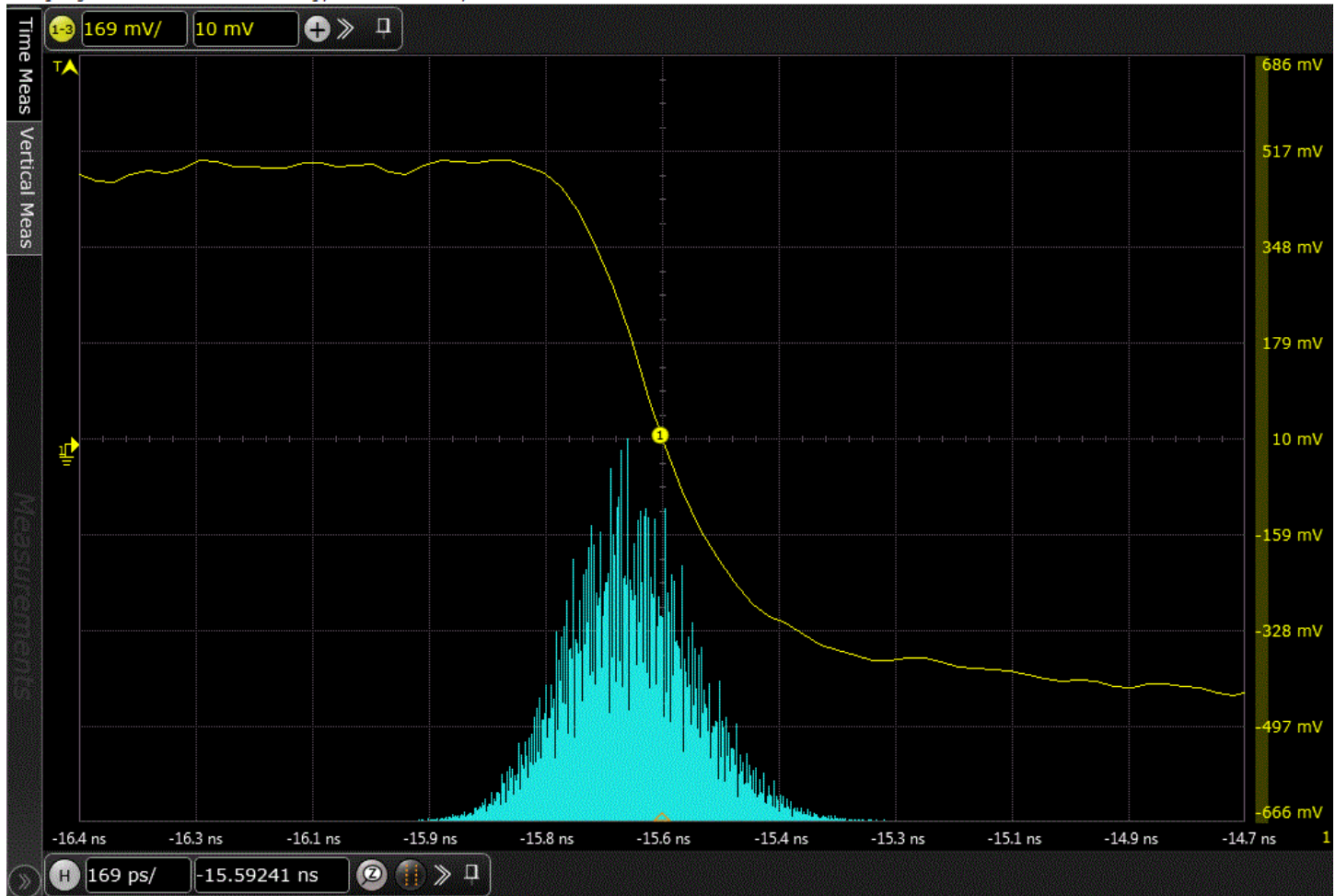
Actual Value Measurement Name: 7-4 Clock Fall Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Upper Threshold(%)	Lower Threshold(%)	VTop(V)	VBase(V)
203.085 ps	170.8	Timing 105	296.694 MHz	80.000	20.000	495 m	-467 m

Upper Threshold(V)	Lower Threshold(V)	# Edges	Acquisition Bandwidth (GHz)
303 m	-275 m	118.678 k	13.000

7-4 Clock Fall Time

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Test ID 7-8

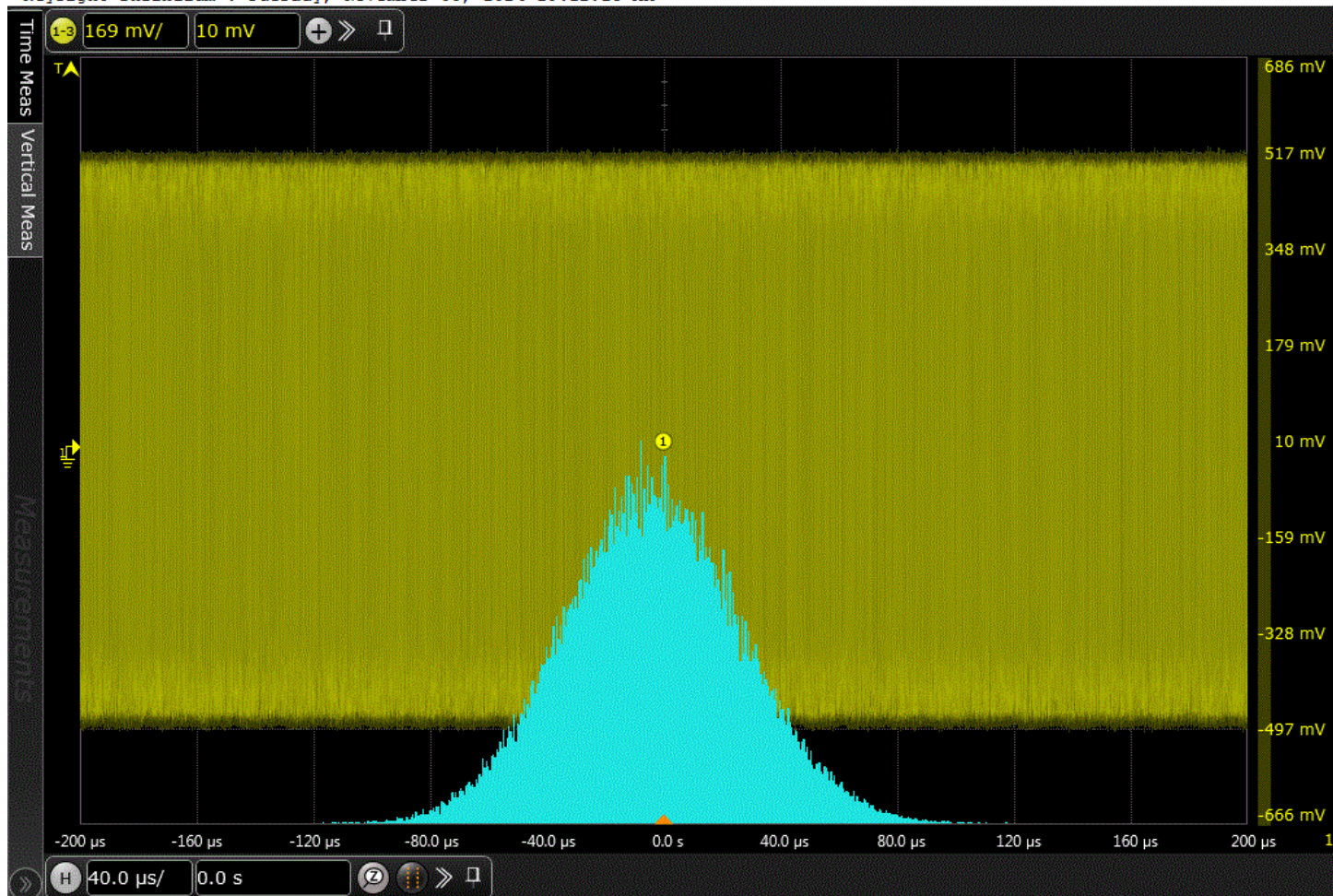
2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-8 Clock Duty Cycle Minimum

Pass Limits: >=40%

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges	TdutyMIN(ns)
49.660	24.2	Timing 105	296.694 MHz	10.000 k	(no value)

7-8 Clock Duty Cycle Minimum

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Test ID 7-8

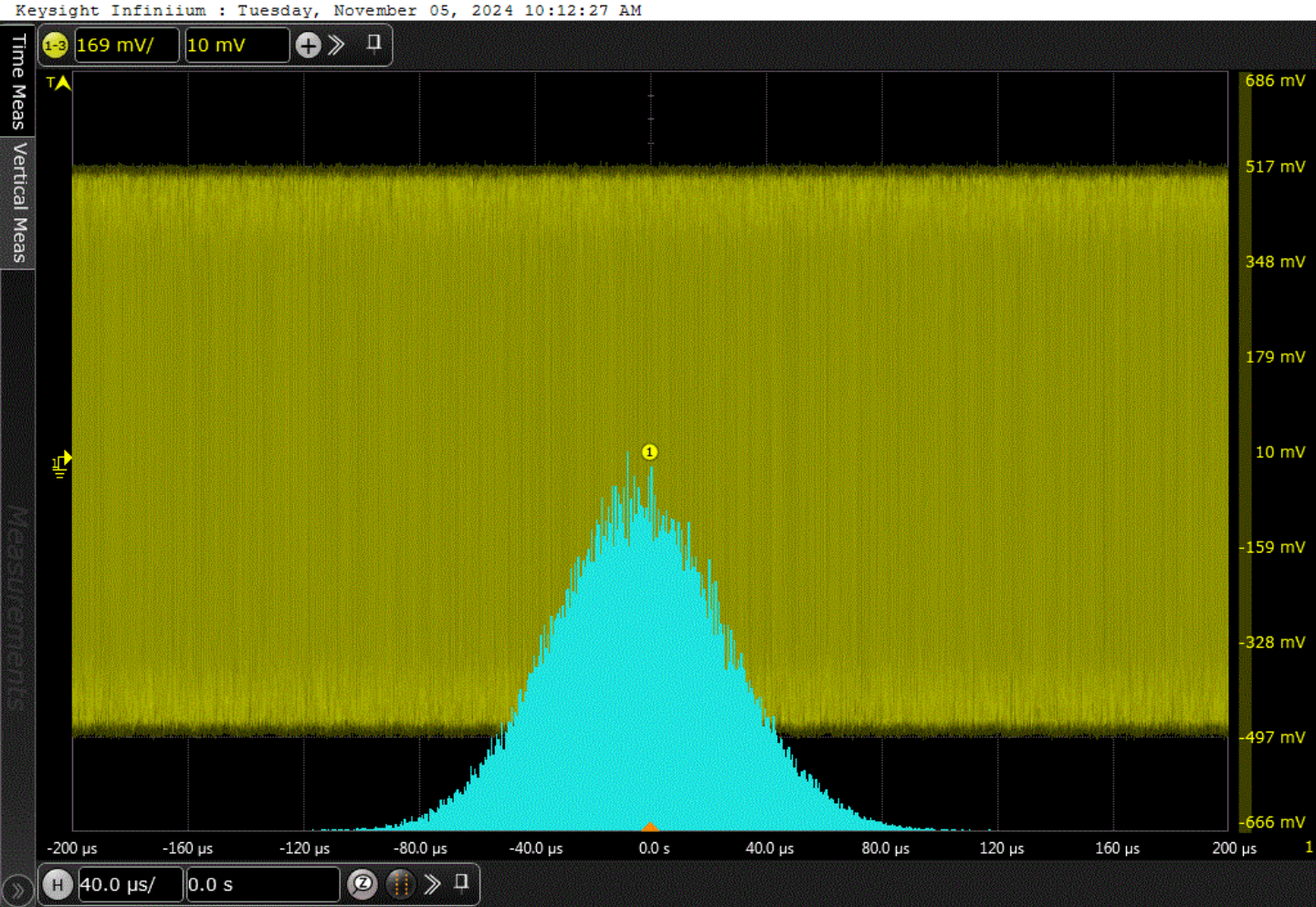
2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-8 Clock Duty Cycle Maximum

Pass Limits: <=60%

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges	TdutyMAX(ns)
50.290	16.2	Timing 105	296.694 MHz	10.000 k	(no value)

7-8 Clock Duty Cycle Maximum



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7-2: VL Clock +

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

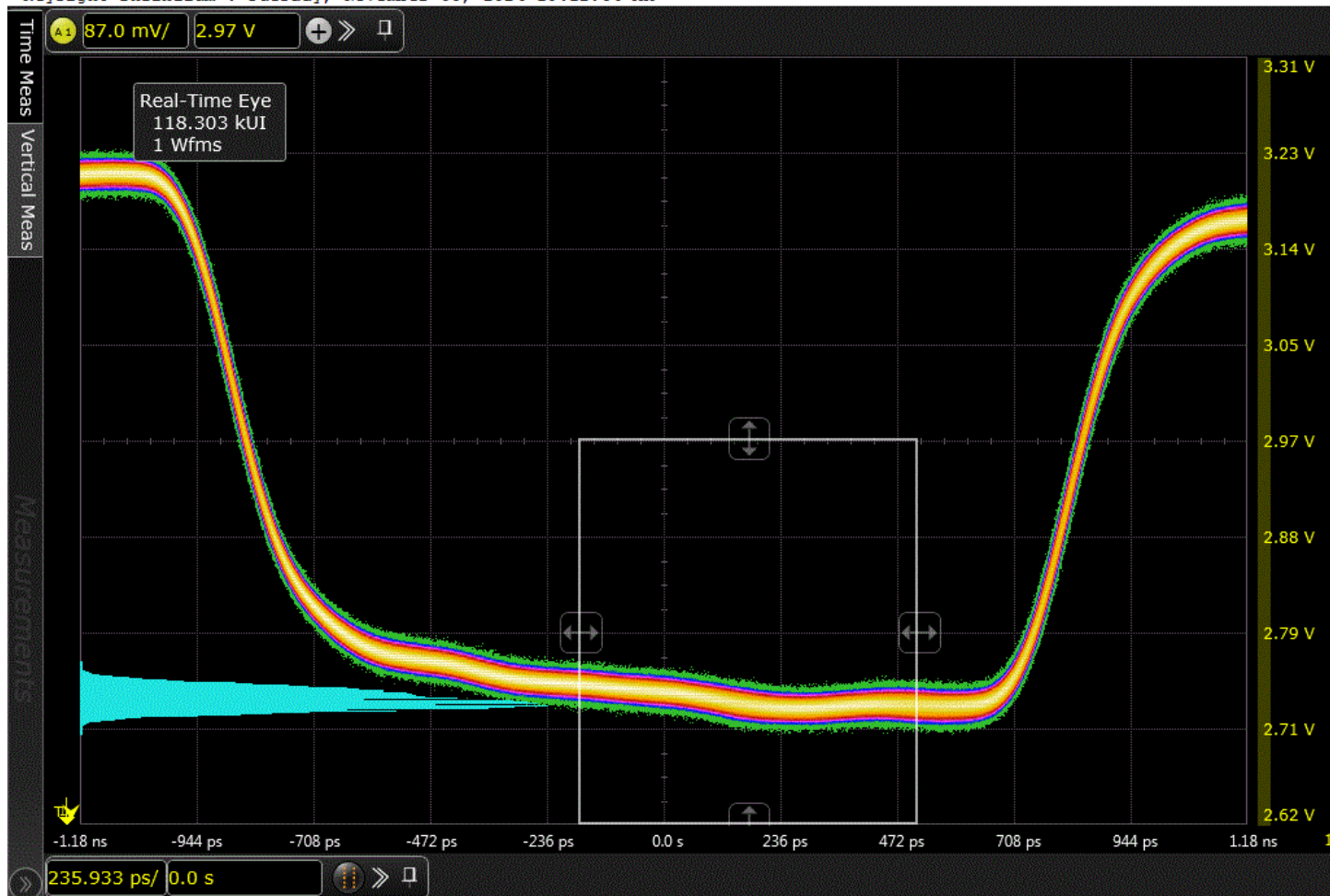
Actual Value Measurement Name: 7-2 VL Clock +

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges	VH	VL
2.765 V	45.0	Timing 105	296.694 MHz	118.303 k	3.245 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-2: VL Clock -

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

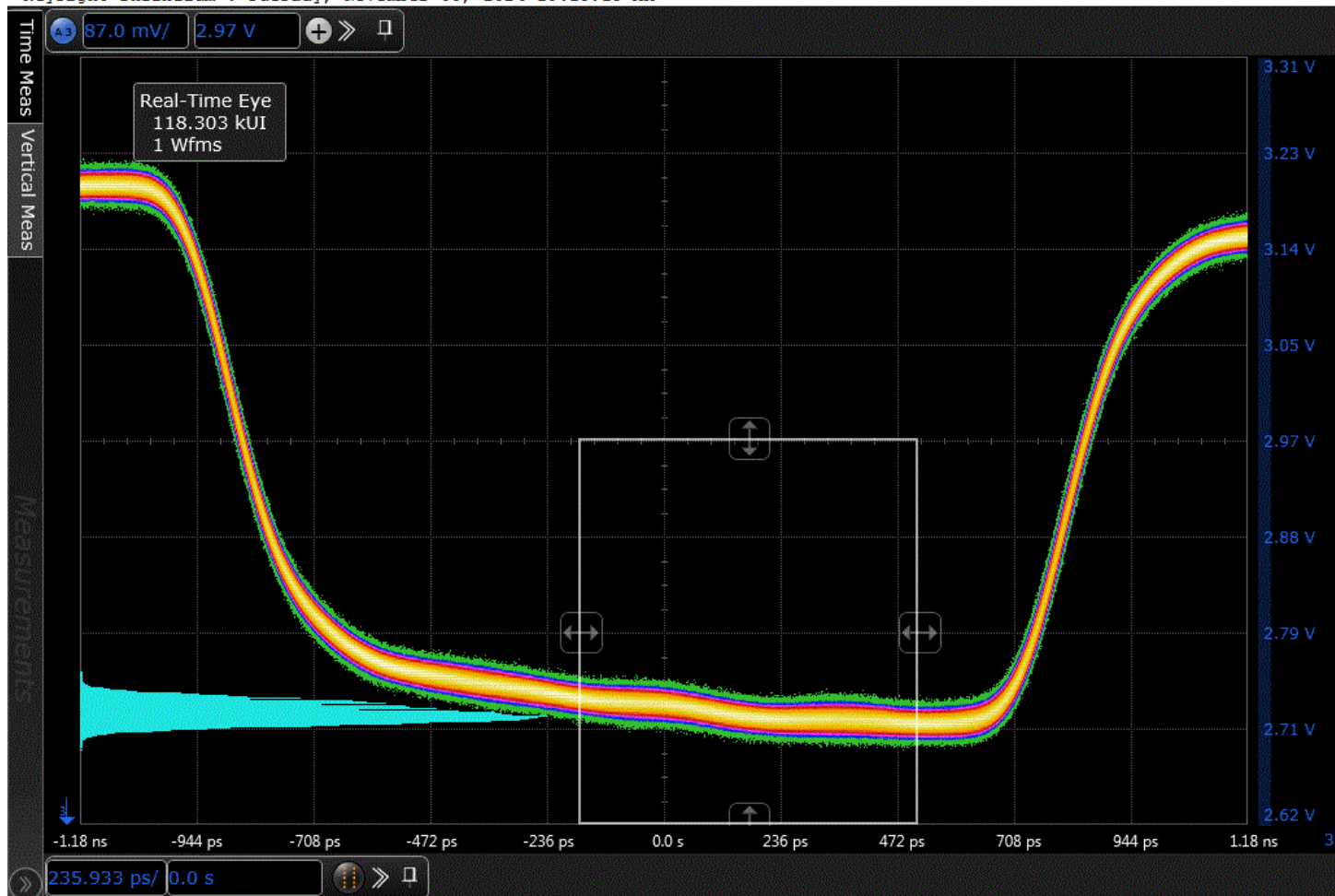
Actual Value Measurement Name: 7-2 VL Clock -

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges	VH	VL
2.768 V	44.0	Timing 105	296.694 MHz	118.303 k	3.244 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-7: Intra-Pair Skew - Clock

Test ID 7-7

Frequency > 165 MHz: Intra-Pair Skew must not exceed $0.15 \times \text{Tbit}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-7 Intra-Pair Skew - Clock

Pass Limits: $-150 \text{ mTbit} \leq \text{VALUE} \leq 150 \text{ mTbit}$

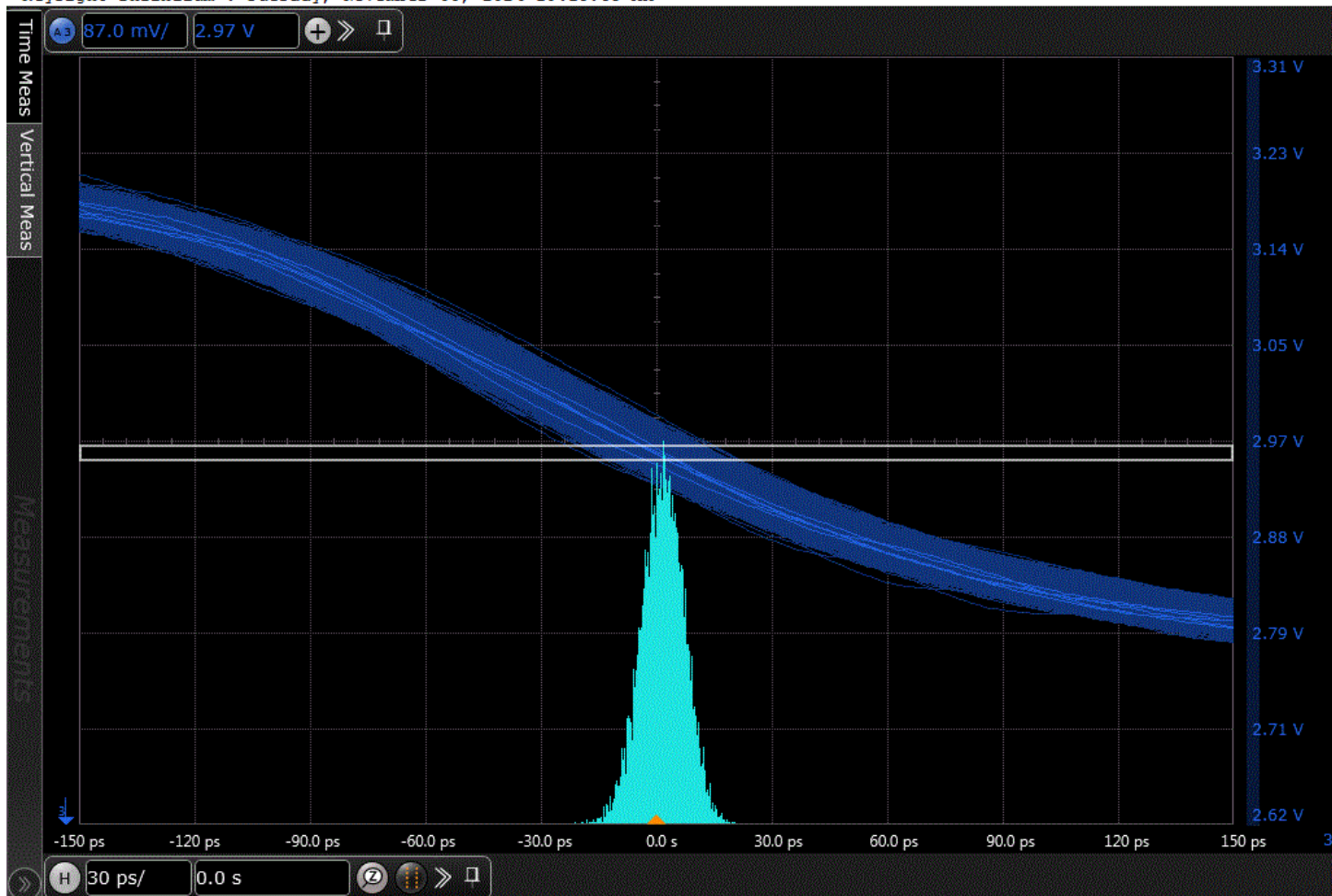
Actual Value	Margin	HDMIAutomationConfig	Max skew (ps)	Min skew (ps)	Mean skew (ps)	Std Dev (ps)	Clk+ threshold (V)
6 mTbit	48.0	Timing 105	20.630	-20.860	1.879	5.455	2.966

Clk- threshold (V)	Acquisition Bandwidth (GHz)	NumEdges	Test Frequency(MHz)	Clock Intra-Pair Skew(ps)
2.955	13.000	12.541000 k	296.694 MHz	2.110

Intra-Pair Skew Distribution

(See image)

Intra-Pair Skew Distribution



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7-10: D0 Mask Test

Test ID 7-10

For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
 Actual Value Measurement Name: 7-10 Total # failures D0 Lane
 Pass Limits: No Mask Failures

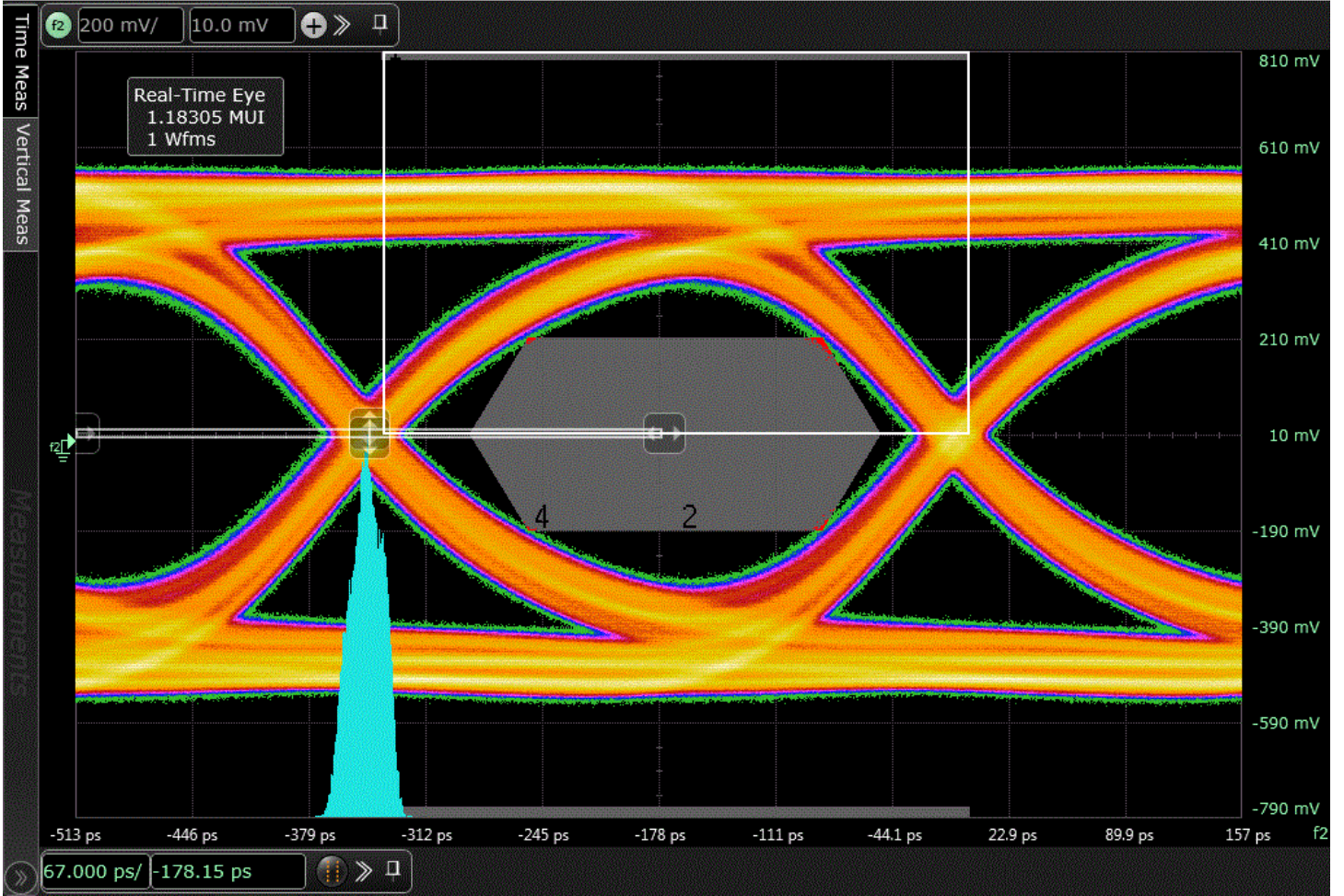
Actual Value	Margin	HDMI Automation Config	Eye Width(ps)	Eye Height(mV)	Data Lane A	Test Frequency(MHz)	Mask Moved(ps)
266.000	-266E+02	Timing 105	282.133	575.000	D0	296.694 MHz	9.750

# Acquisitions	Point	Tbit(ps)	RightJitterData(Tbit)	LeftJitterData(Tbit)	RightJitterData(ps)	LeftJitterData(ps)	Maximum Margin
16000000		337.051	163.064 m	163.064 m	54.961	54.961	NA

Left Margin	Right Margin	Maximum Margin (Vertical)	Upper Margin (Vertical)	Lower Margin (Vertical)
NA	NA	NA	NA	NA

Differential Swing Voltage, VH(V)	Differential Swing Voltage, VL (V)	Differential Swing Voltage(V)	Acquisition Bandwidth (GHz)
525 m	-502 m	1.027	13.000

7-10 Total # failures D0 Lane



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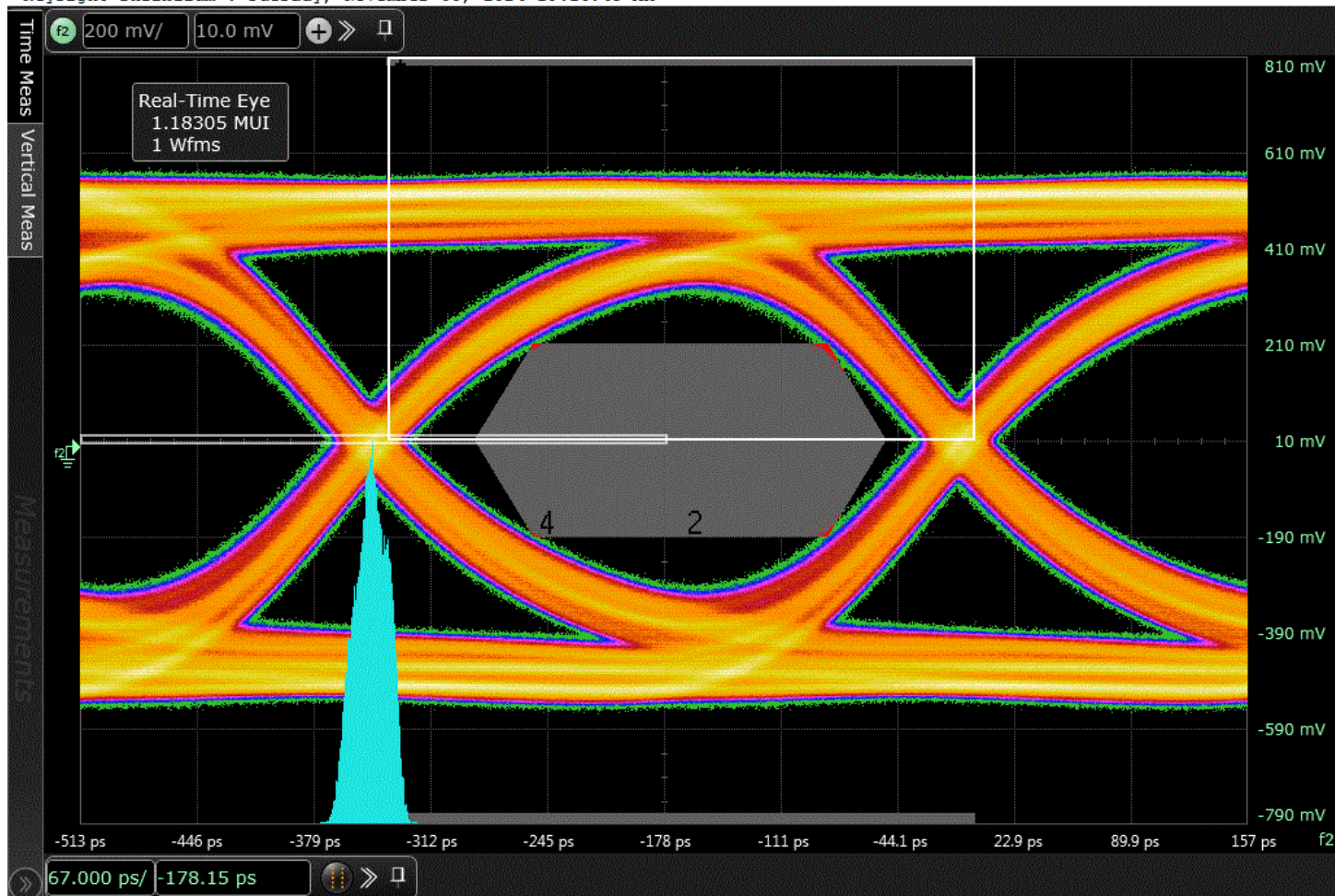
7-10: D0 Data Jitter

Test ID 7-10

For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
Actual Value Measurement Name: 7-10 D0 Data Jitter
Pass Limits: <=0.3Tbit

Actual Value	Margin	HDMIAutomationConfig
163 m	45.7	Timing 105

7-10 D0 Data Jitter

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7-4: D0 Rise Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

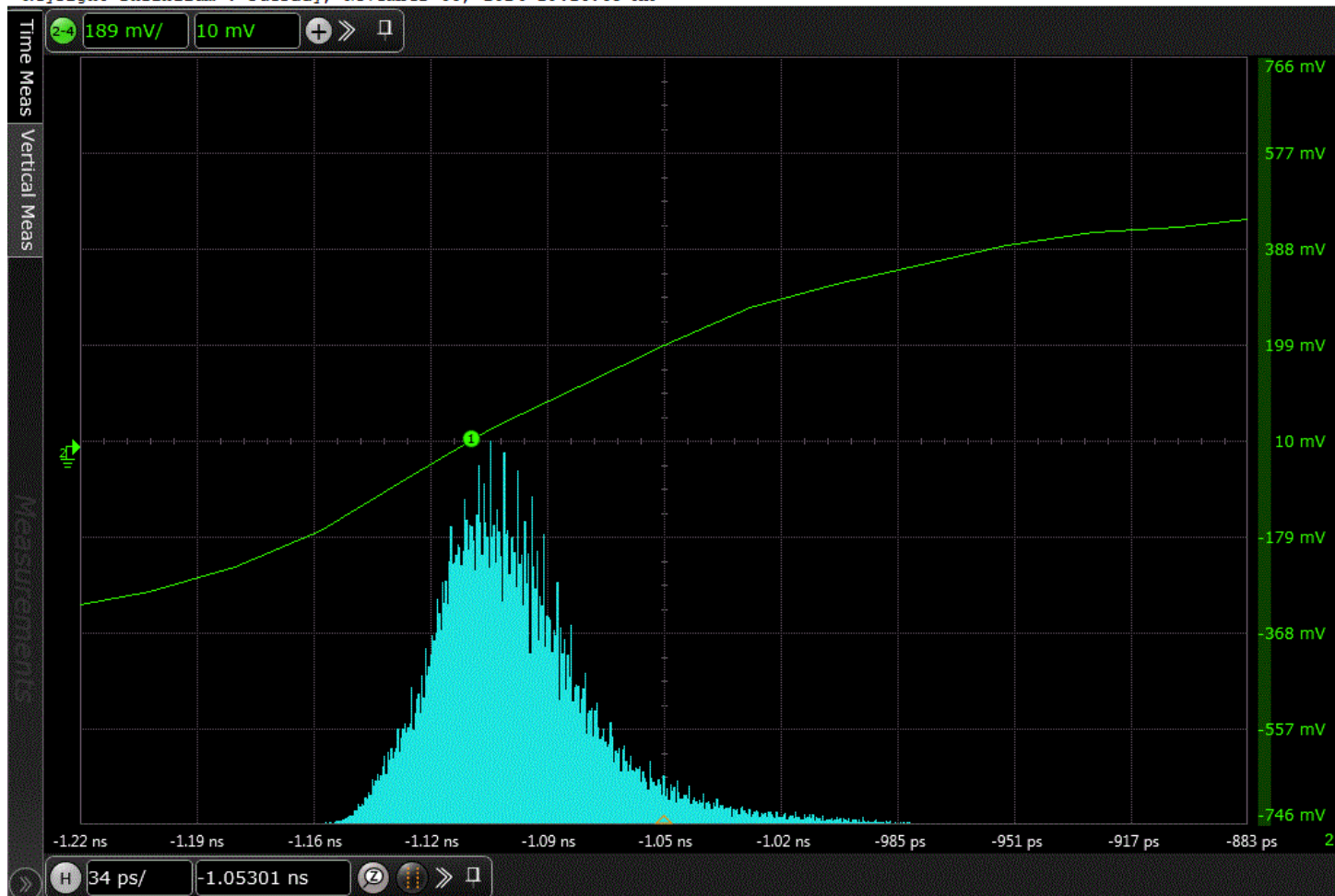
Actual Value Measurement Name: 7-4 D0 Rise Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Edge Type	Upper Threshold(%)	Lower Threshold(%)
191.527 ps	155.4	Timing 105	296.694 MHz	D0	All edges	80.000	20.000

VTop(V)	VBase(V)	Upper Threshold(V)	Lower Threshold(V)	#Edge	Acquisition Bandwidth (GHz)
525 m	-502 m	320 m	-297 m	234.445 k	13.000

7-4 D0 Rise Time



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7-4: D0 Fall Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

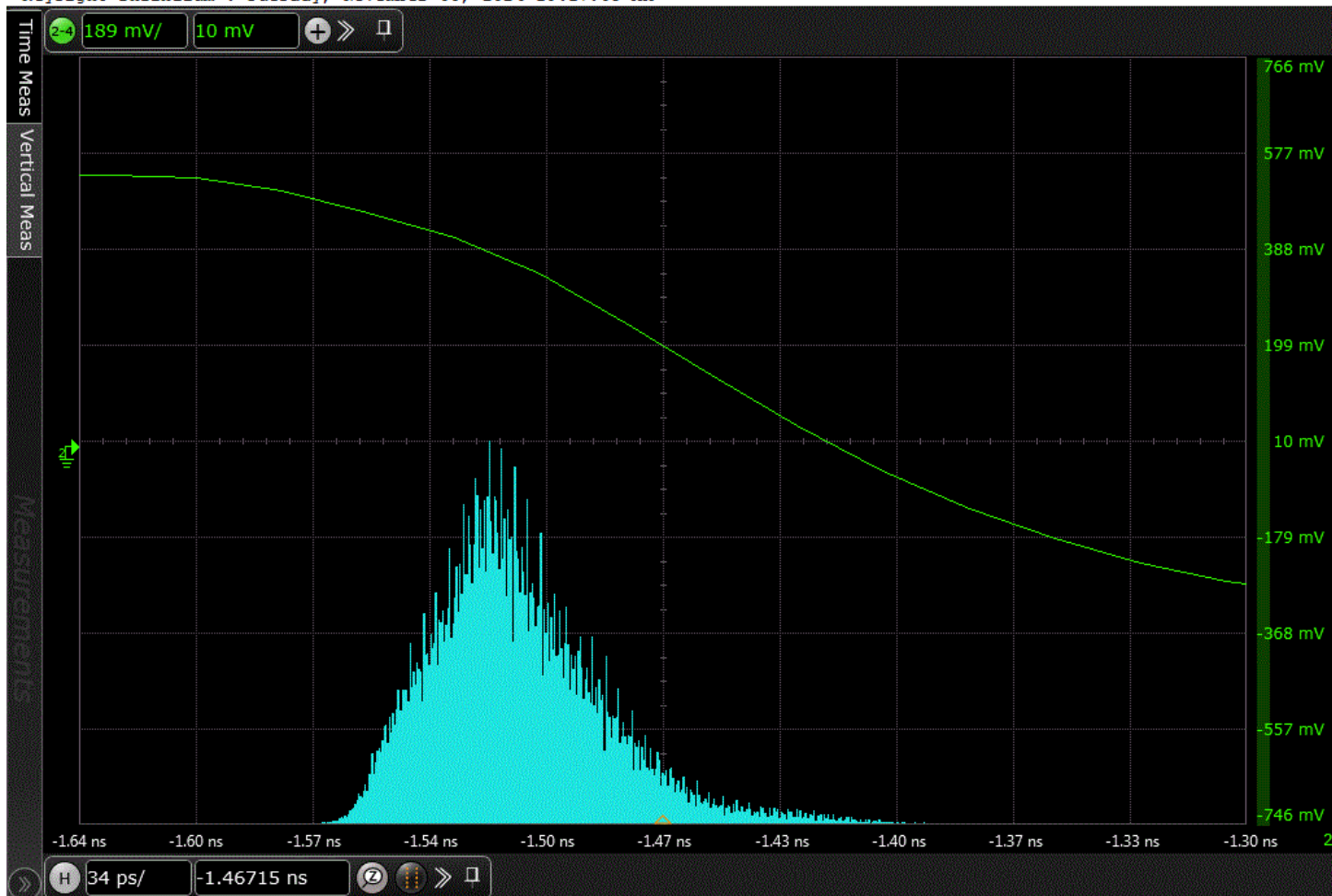
Actual Value Measurement Name: 7-4 D0 Fall Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Edge Type	Upper Threshold(%)	Lower Threshold(%)
191.027 ps	154.7	Timing 105	296.694 MHz	D0	All edges	80.000	20.000

VTop(V)	VBase(V)	Upper Threshold(V)	Lower Threshold(V)	#Edge	Acquisition Bandwidth (GHz)
525 m	-502 m	320 m	-297 m	234.444 k	13.000

7-4 D0 Fall Time

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7-2: VL D0+

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

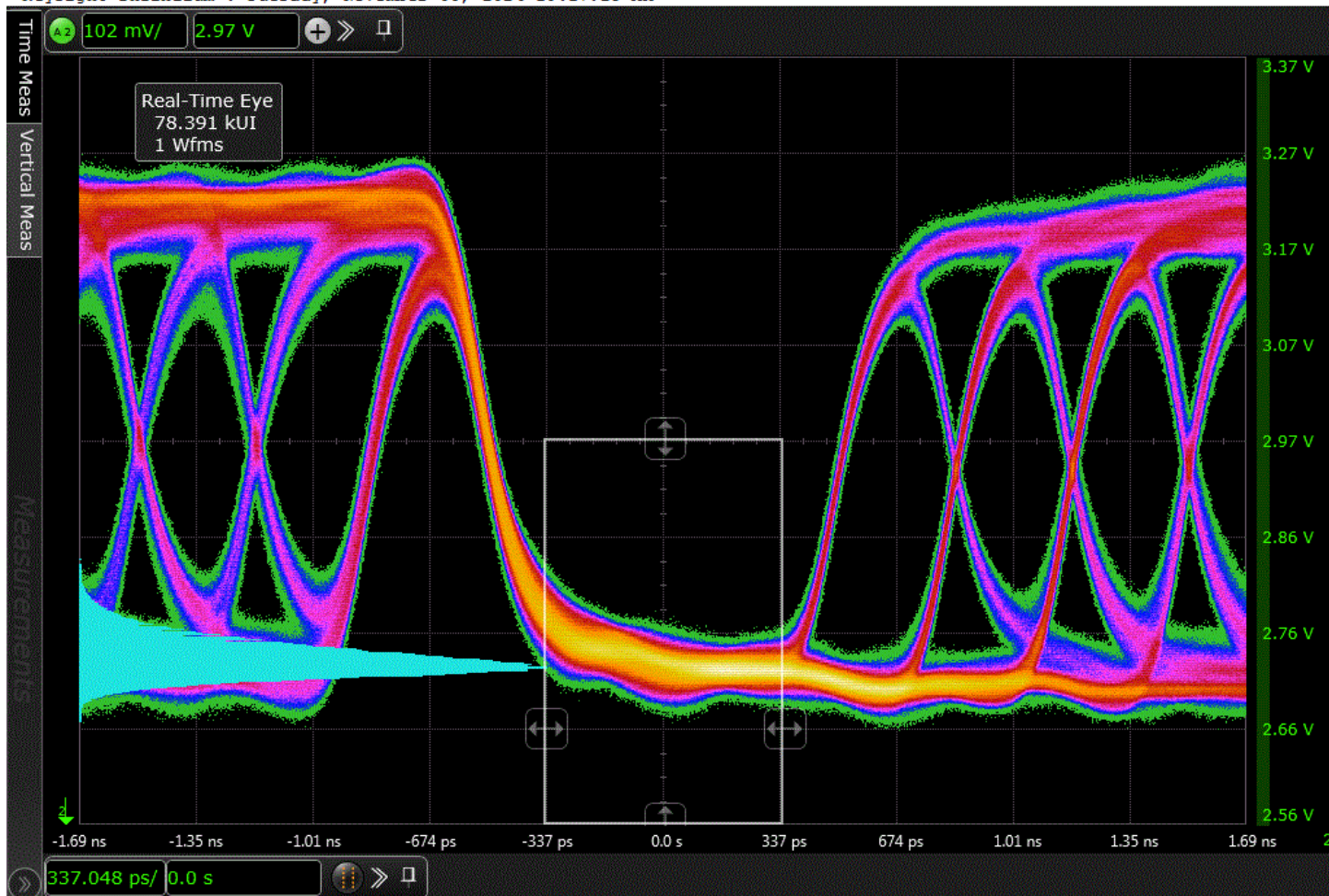
Actual Value Measurement Name: 7-2 VL D0+

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.766 V	44.7	Timing 105	296.694 MHz	78.391 k	72.214 k	3.238 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL


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7-2: VL D0-

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

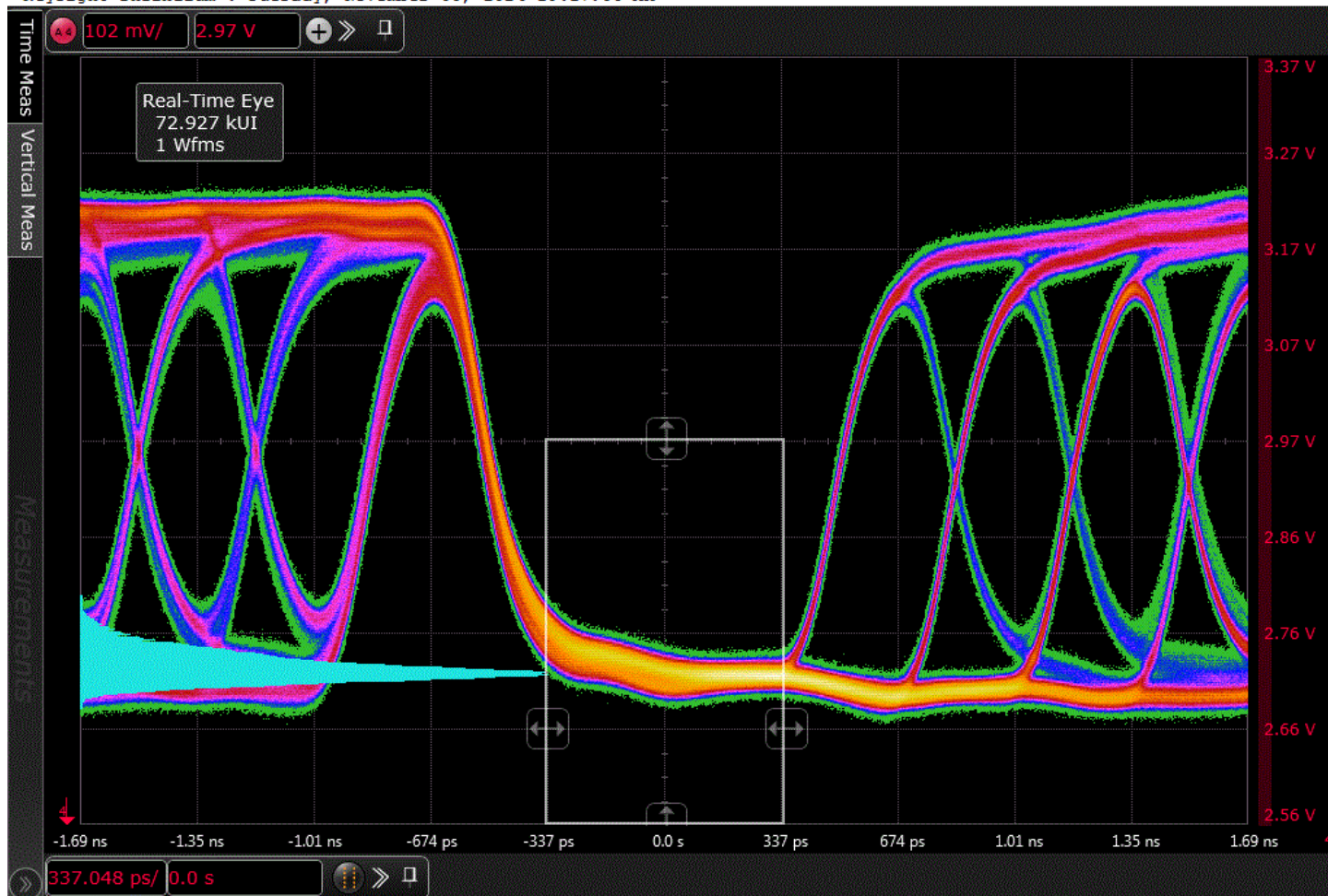
Actual Value Measurement Name: 7-2 VL D0-

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.771 V	43.0	Timing 105	296.694 MHz	72.927 k	76.282 k	3.240 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-7: Intra-Pair Skew - Data Lane 0

Test ID 7-7

Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-7 Intra-Pair Skew - D0 Lane

Pass Limits: -150 mTbit <= VALUE <= 150 mTbit

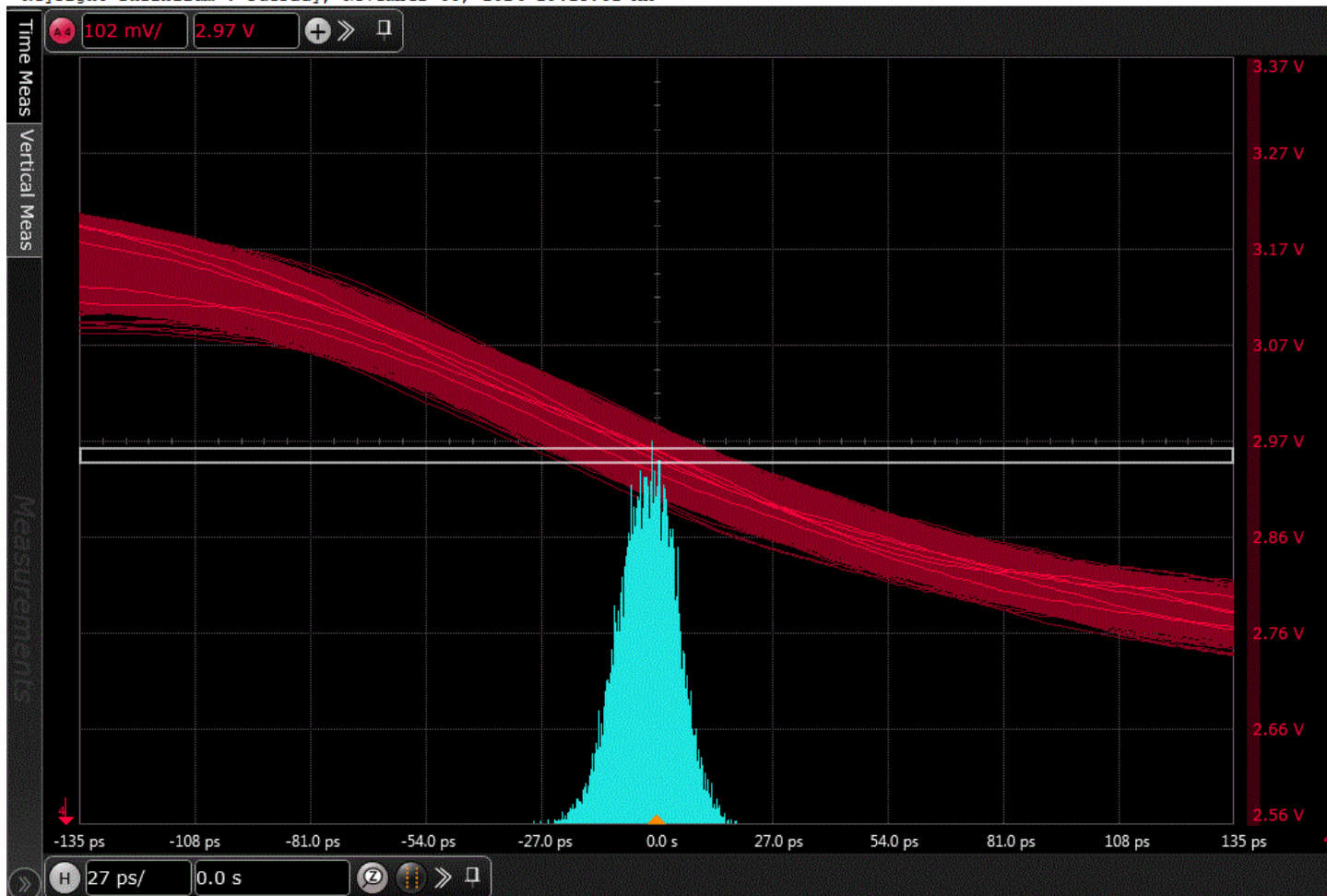
Actual Value	Margin	HDMIAutomationConfig	Max skew (ps)	Min skew (ps)	Mean skew (ps)	Std Dev (ps)	D+ threshold (V)
-3 mTbit	49.0	Timing 105	18.770	-28.480	-1.987	6.595	2.962

D- threshold (V)	Acquisition Bandwidth (GHz)	NumEdges	Test Frequency(MHz)	Data Intra-Pair Skew(ps)
2.951	13.000	13.870000 k	296.694 MHz	-1.050

Intra-Pair Skew Distribution

(See image)

Intra-Pair Skew Distribution



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7-10: D1 Mask Test

Test ID 7-10

For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
 Actual Value Measurement Name: 7-10 Total # failures D1 lane
 Pass Limits: No Mask Failures

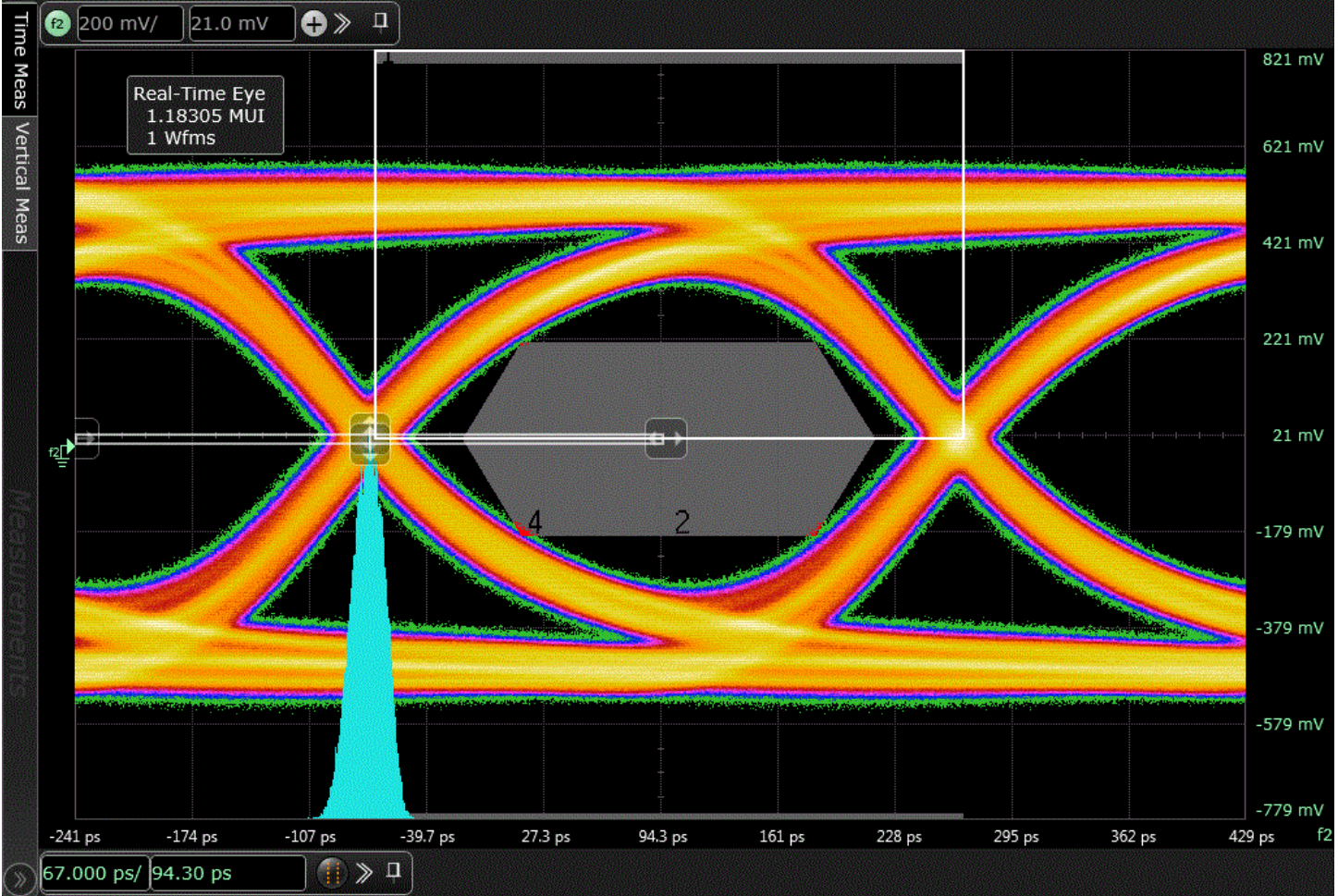
Actual Value	Margin	HDMI Automation Config	Eye Width(ps)	Eye Height(mV)	Data Lane A	Test Frequency(MHz)	Mask Moved(ps)
204.000	-204E+02	Timing 105	276.375	591.000	D1	296.694 MHz	4.870

# Acquisitions	Point	Tbit(ps)	RightJitterData(Tbit)	LeftJitterData(Tbit)	RightJitterData(ps)	LeftJitterData(ps)	Maximum Margin
16000000		337.048	180.149 m	180.149 m	60.719	60.719	NA

Left Margin	Right Margin	Maximum Margin (Vertical)	Upper Margin (Vertical)	Lower Margin (Vertical)
NA	NA	NA	NA	NA

Differential Swing Voltage, VH(V)	Differential Swing Voltage, VL (V)	Differential Swing Voltage(V)	Acquisition Bandwidth (GHz)
496 m	-451 m	947 m	13.000

7-10 Total # failures D1 lane



7-10: D1 Data Jitter

Test ID 7-10

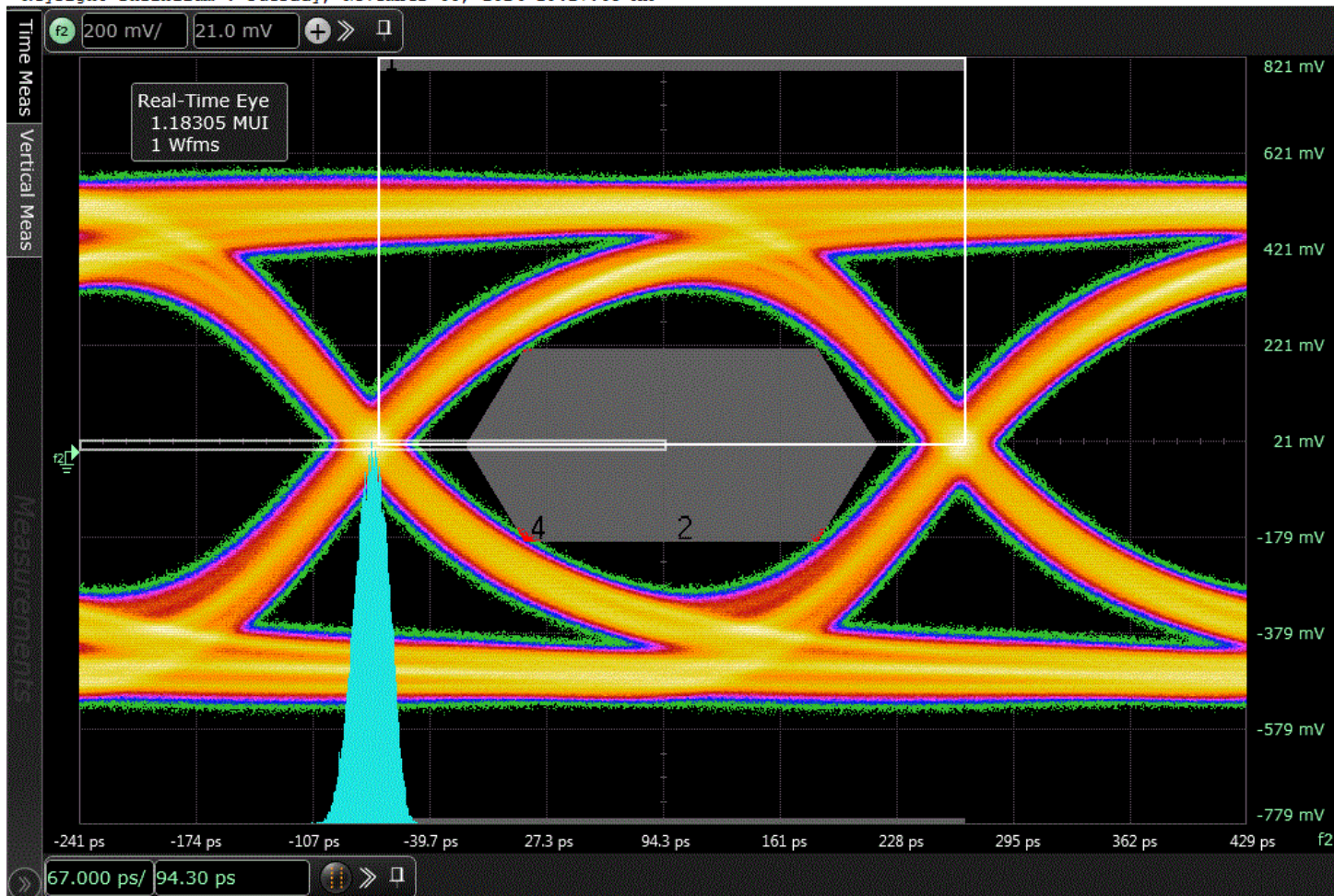
For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Actual Value Measurement Name: 7-10 D1 Data Jitter

Pass Limits: <=0.3Tbit

Actual Value	Margin	HDMIAutomationConfig
180 m	40.0	Timing 105

7-10 D1 Data Jitter



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7-4: D1 Rise Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

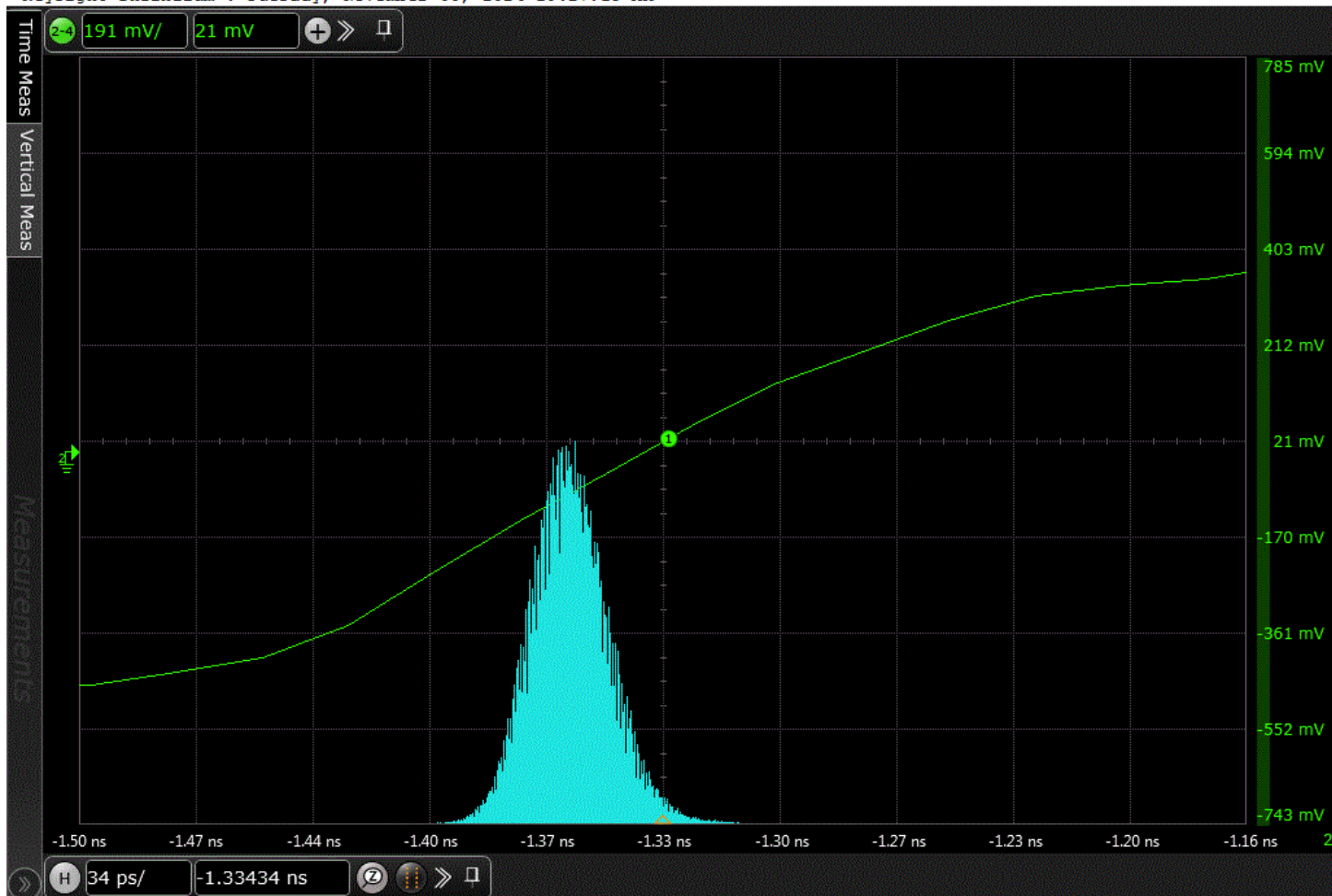
Actual Value Measurement Name: 7-4 D1 Rise Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Edge Type	Upper Threshold(%)	Lower Threshold(%)
170.902 ps	127.9	Timing 105	296.694 MHz	D1	All edges	80.000	20.000

VTop(V)	VBase(V)	Upper Threshold(V)	Lower Threshold(V)	#Edge	Acquisition Bandwidth (GHz)
496 m	-451 m	307 m	-262 m	271.931 k	13.000

7-4 D1 Rise Time

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7-4: D1 Fall Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

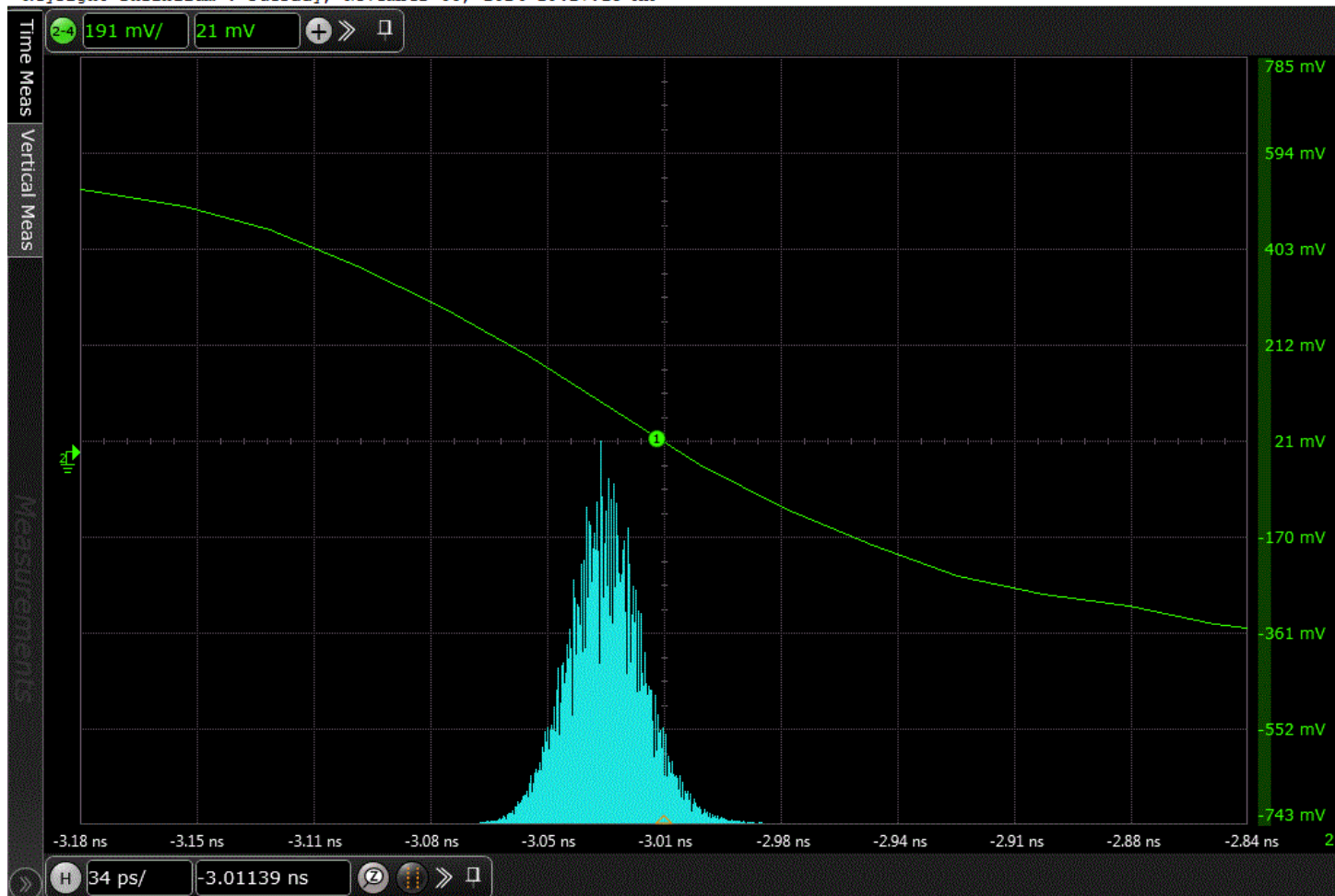
Actual Value Measurement Name: 7-4 D1 Fall Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Edge Type	Upper Threshold(%)	Lower Threshold(%)
167.269 ps	123.0	Timing 105	296.694 MHz	D1	All edges	80.000	20.000

VTop(V)	VBase(V)	Upper Threshold(V)	Lower Threshold(V)	#Edge	Acquisition Bandwidth (GHz)
496 m	-451 m	307 m	-262 m	271.931 k	13.000

7-4 D1 Fall Time

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7-2: VL D1+

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

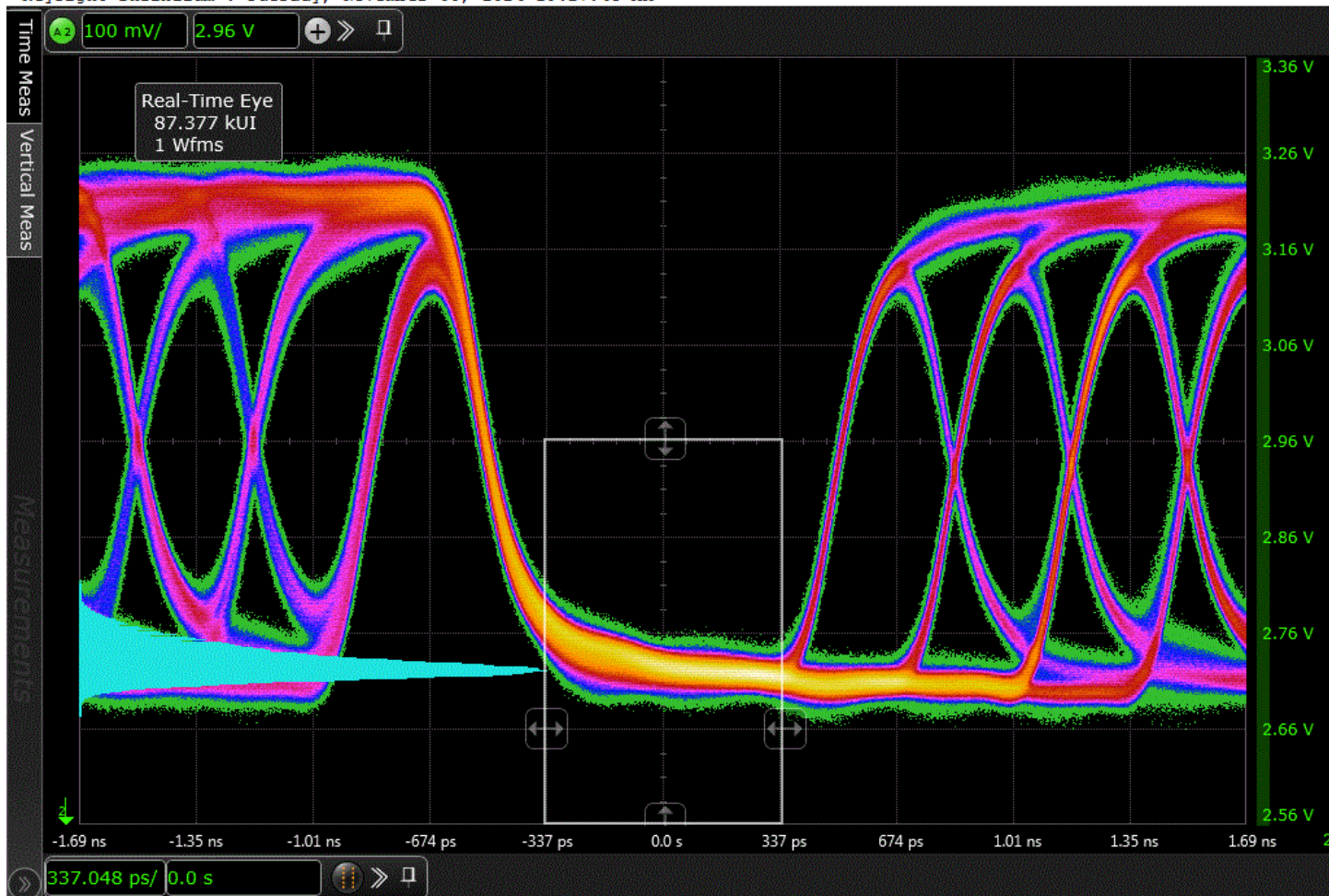
Actual Value Measurement Name: 7-2 VL D1+

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.764 V	45.3	Timing 105	296.694 MHz	87.377 k	71.963 k	3.240 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-2: VL D1-

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

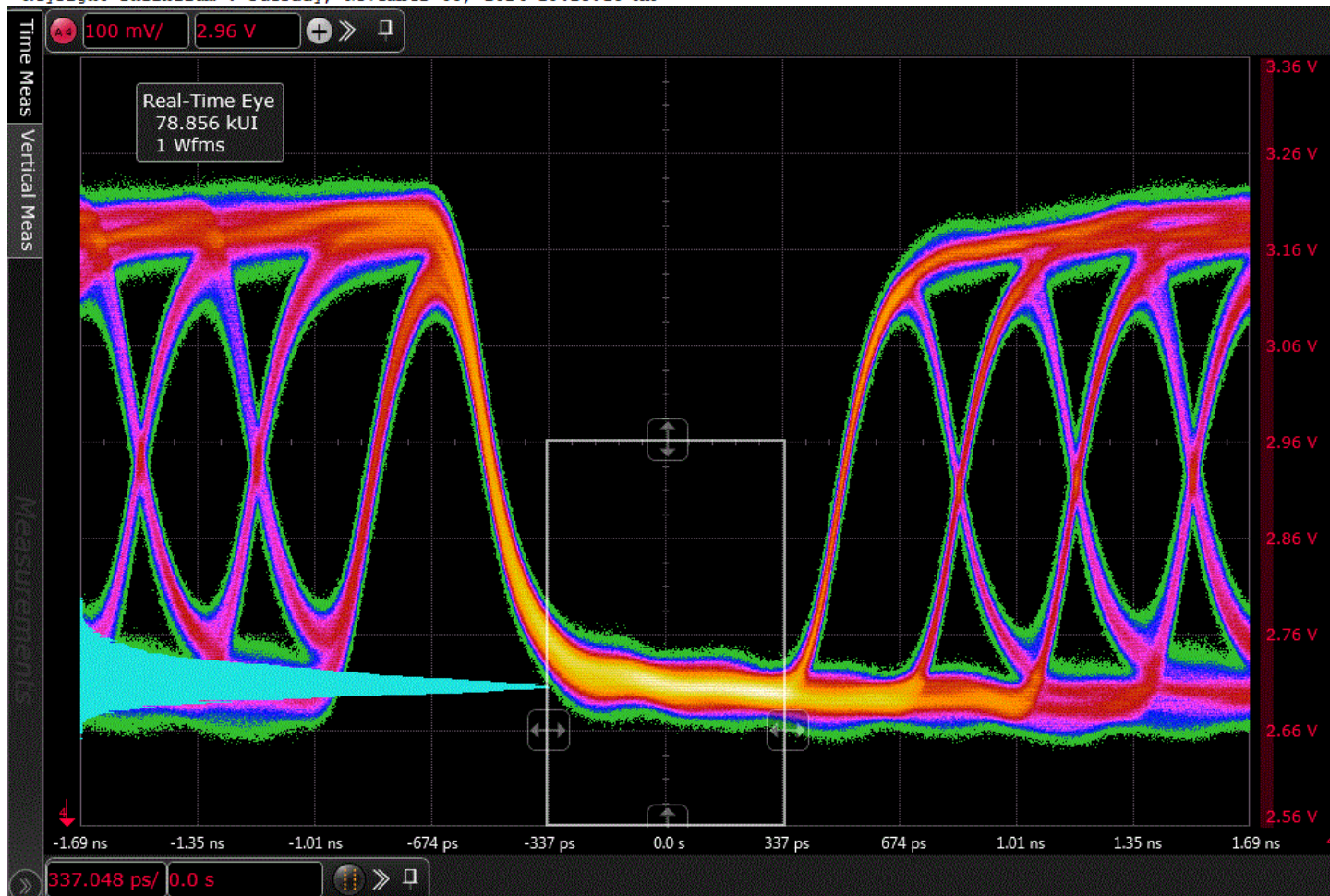
Actual Value Measurement Name: 7-2 VL D1-

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.763 V	45.7	Timing 105	296.694 MHz	78.856 k	88.495 k	3.234 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-7: Intra-Pair Skew - Data Lane 1

Test ID 7-7

Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-7 Intra-Pair Skew - D1 Lane

Pass Limits: -150 mTbit <= VALUE <= 150 mTbit

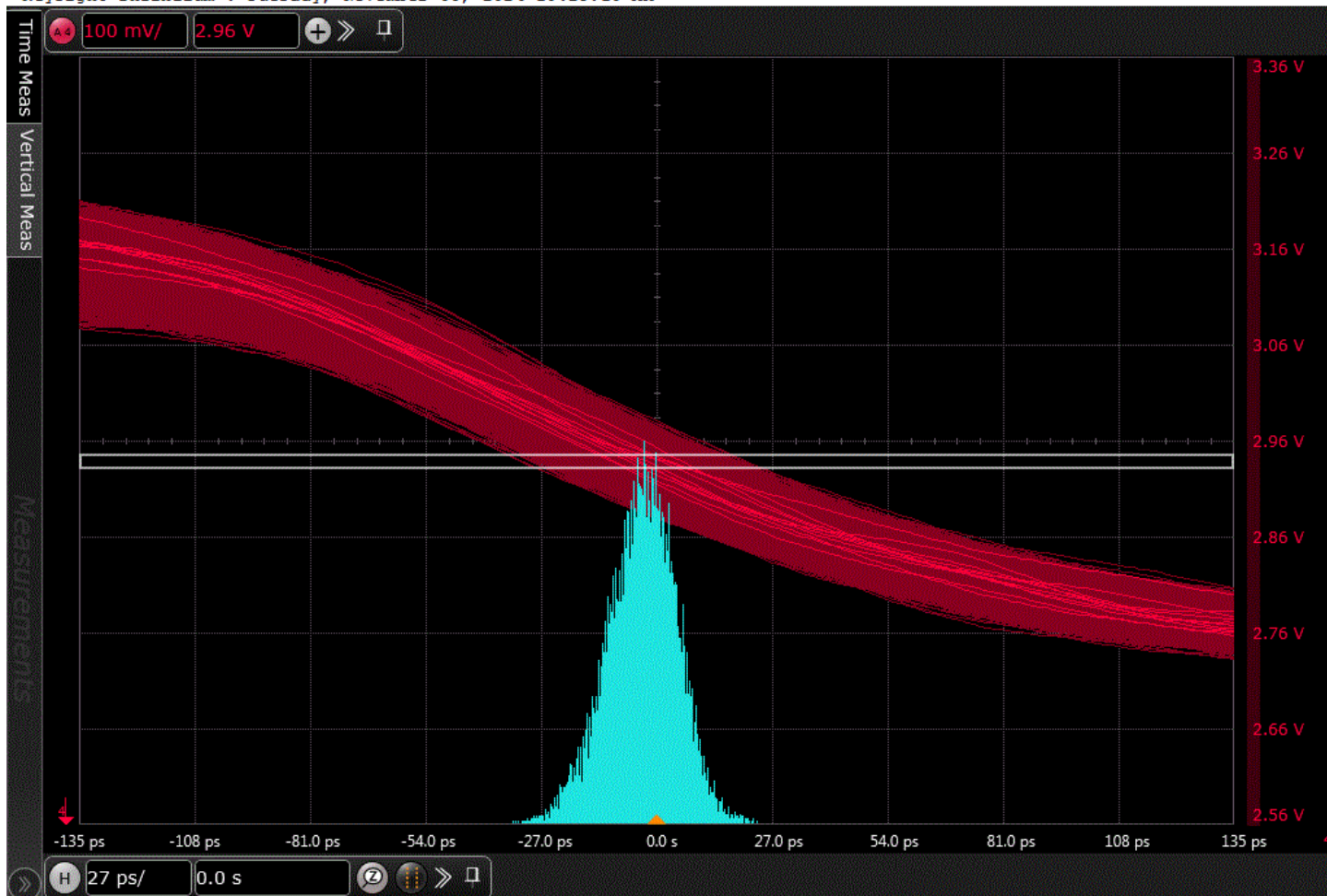
Actual Value	Margin	HDMIAutomationConfig	Max skew (ps)	Min skew (ps)	Mean skew (ps)	Std Dev (ps)	D+ threshold (V)
-8 mTbit	47.3	Timing 105	23.840	-33.540	-3.300	8.008	2.963

D- threshold (V)	Acquisition Bandwidth (GHz)	NumEdges	Test Frequency(MHz)	Data Intra-Pair Skew(ps)
2.943	13.000	13.029000 k	296.694 MHz	-2.740

Intra-Pair Skew Distribution

(See image)

Intra-Pair Skew Distribution



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7-10: D2 Mask Test

Test ID 7-10

For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Actual Value Measurement Name: 7-10 Total # failures D2 Lane

Pass Limits: No Mask Failures

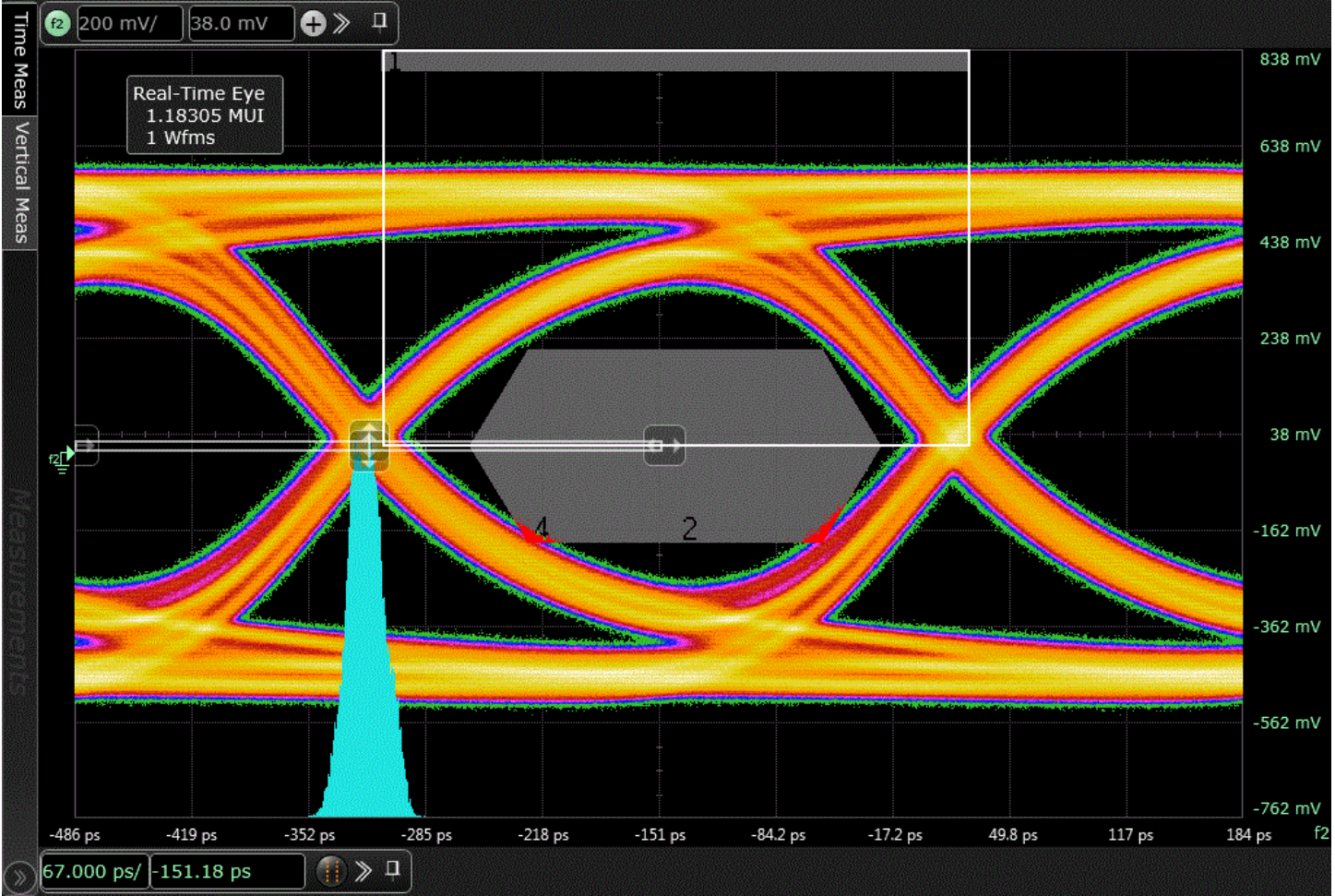
Actual Value	Margin	HDMI Automation Config	Eye Width(ps)	Eye Height(mV)	Data Lane A	Test Frequency(MHz)	Mask Moved(ps)
4.090000 k	-409E+03	Timing 105	270.617	570.000	D2	296.694 MHz	9.750

# Acquisitions	Point	Tbit(ps)	RightJitterData(Tbit)	LeftJitterData(Tbit)	RightJitterData(ps)	LeftJitterData(ps)	Maximum Margin
16000000		337.048	197.232 m	197.232 m	66.477	66.477	NA

Left Margin	Right Margin	Maximum Margin (Vertical)	Upper Margin (Vertical)	Lower Margin (Vertical)
NA	NA	NA	NA	NA

Differential Swing Voltage, VH(V)	Differential Swing Voltage, VL (V)	Differential Swing Voltage(V)	Acquisition Bandwidth (GHz)
558 m	-485 m	1.043	13.000

7-10 Total # failures D2 Lane



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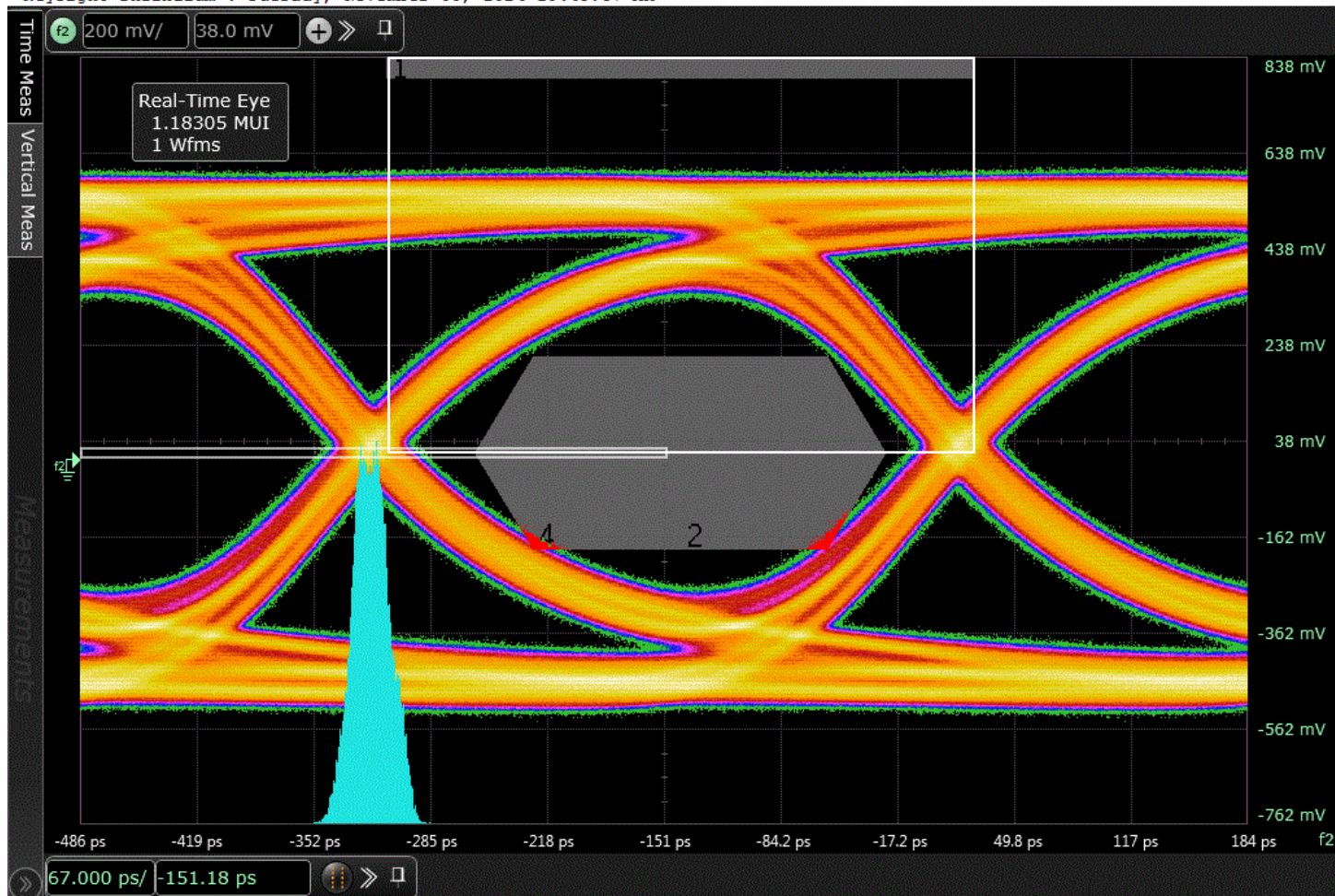
7-10: D2 Data Jitter

Test ID 7-10

For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
Actual Value Measurement Name: 7-10 D2 Data Jitter
Pass Limits: <=0.3Tbit

Actual Value	Margin	HDMIAutomationConfig
197 m	34.3	Timing 105

7-10 D2 Data Jitter



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7-4: D2 Rise Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

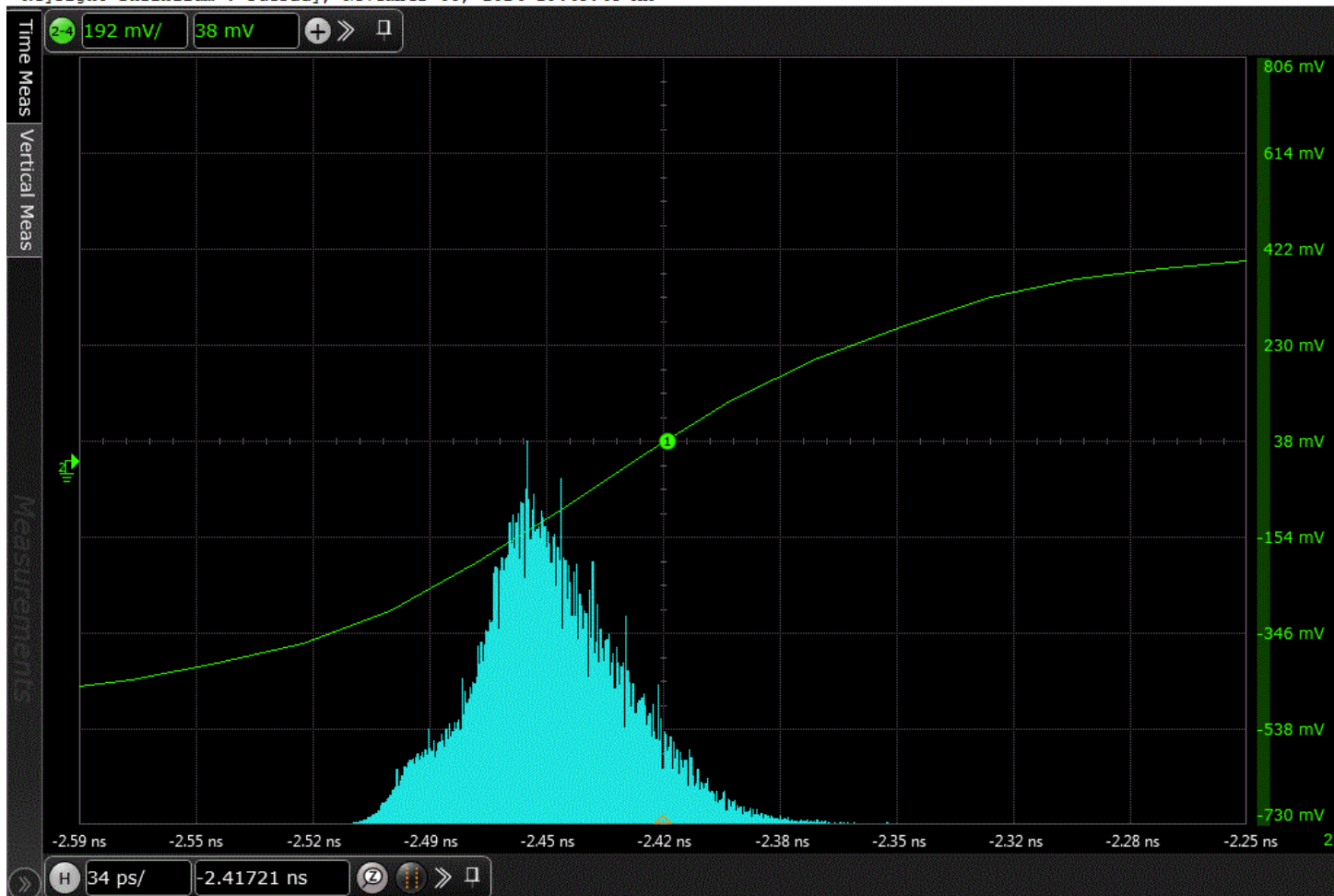
Actual Value Measurement Name: 7-4 D2 Rise Time

Pass Limits: VALUE \geq 75.000 ps

Actual Value	Margin	HDMI Automation Config	Test Frequency (MHz)	Data Lane A	Edge Type	Upper Threshold (%)	Lower Threshold (%)
200.390 ps	167.2	Timing 105	296.694 MHz	D2	All edges	80.000	20.000

VTop (V)	VBase (V)	Upper Threshold (V)	Lower Threshold (V)	#Edge	Acquisition Bandwidth (GHz)
558 m	-485 m	349 m	-276 m	246.812 k	13.000

7-4 D2 Rise Time

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7-4: D2 Fall Time

Test ID 7-4

The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

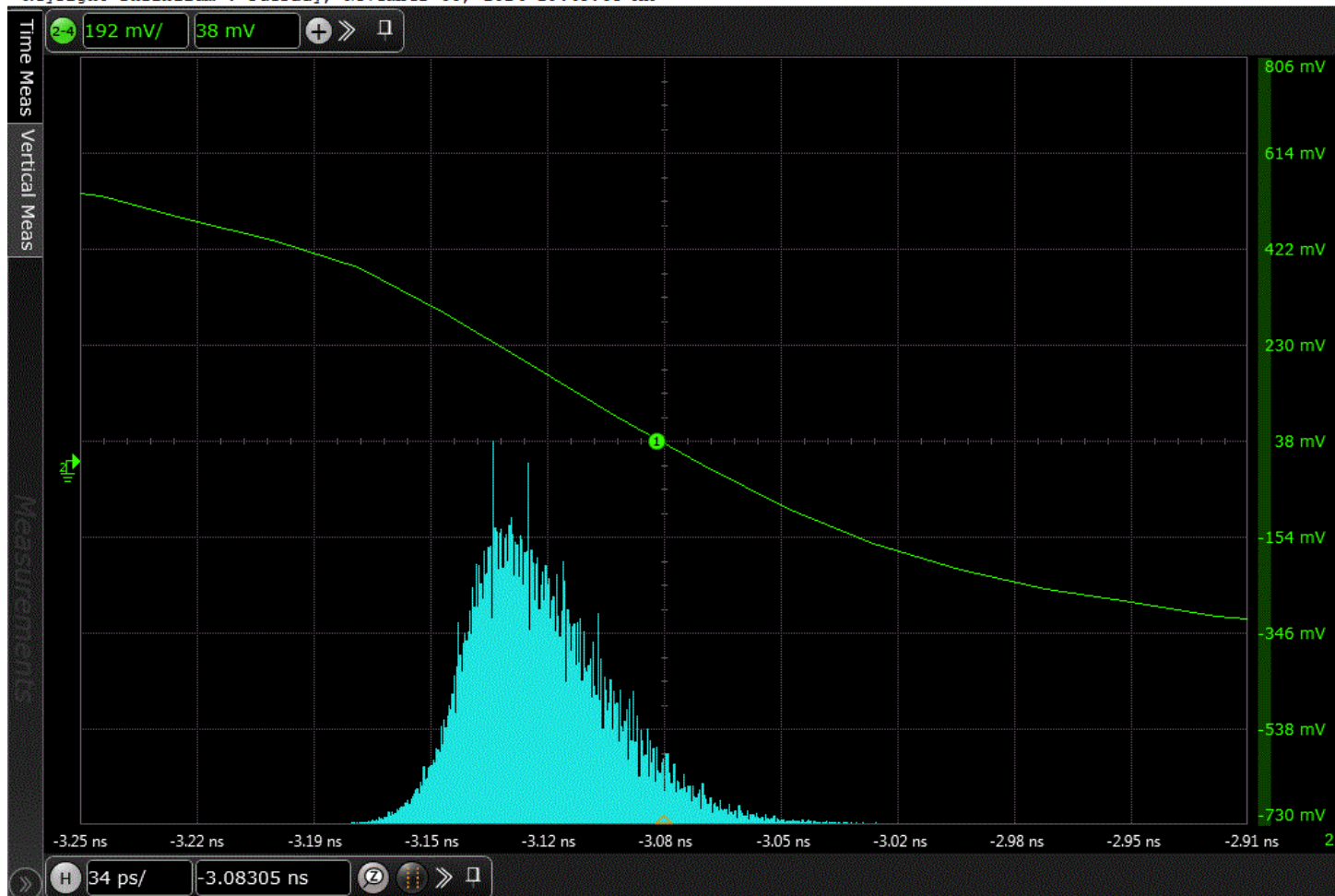
Actual Value Measurement Name: 7-4 D2 Fall Time

Pass Limits: VALUE >= 75.000 ps

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Edge Type	Upper Threshold(%)	Lower Threshold(%)
197.005 ps	162.7	Timing 105	296.694 MHz	D2	All edges	80.000	20.000

VTop(V)	VBase(V)	Upper Threshold(V)	Lower Threshold(V)	#Edge	Acquisition Bandwidth (GHz)
558 m	-485 m	349 m	-276 m	246.812 k	13.000

7-4 D2 Fall Time

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7-2: VL D2+

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

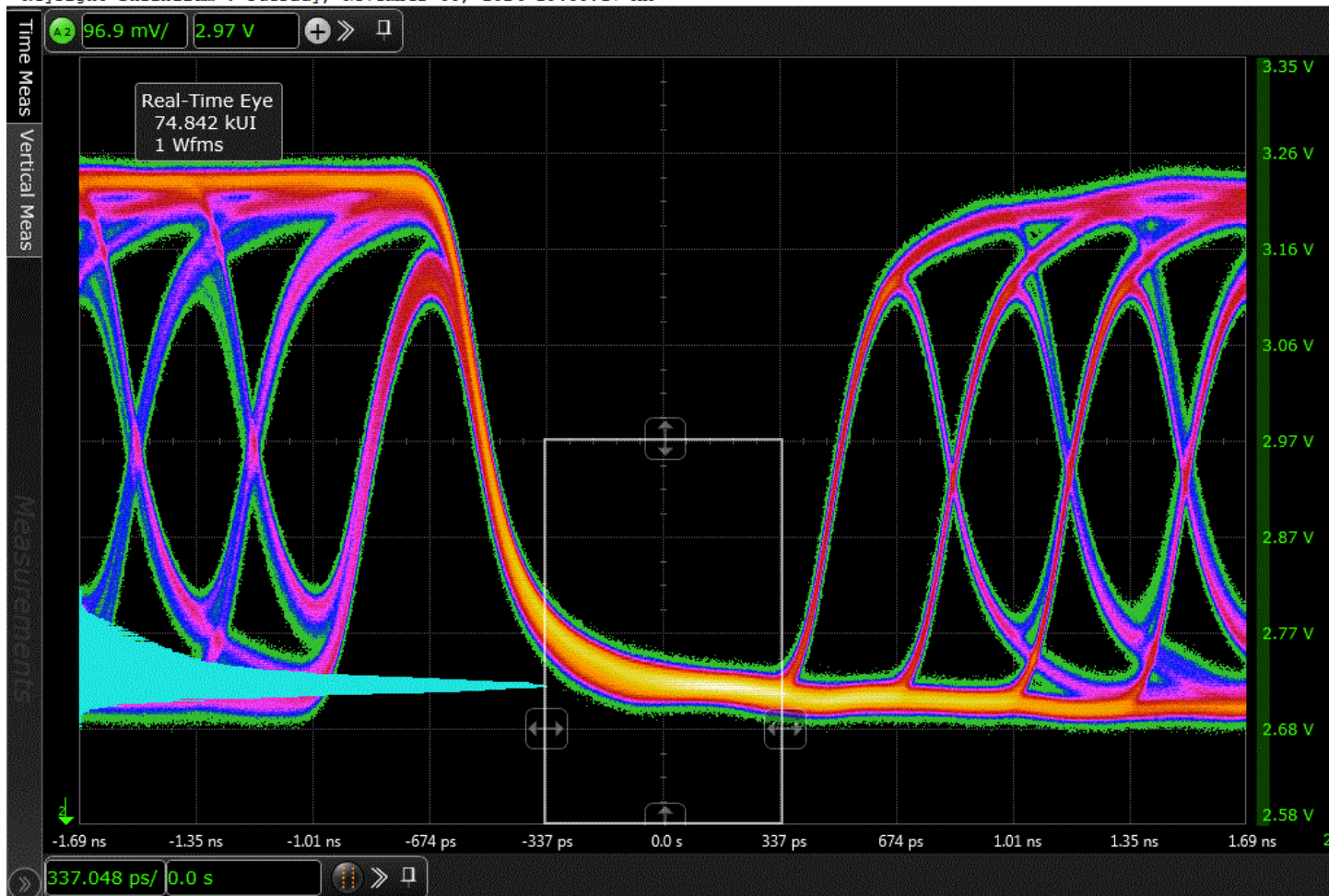
Actual Value Measurement Name: 7-2 VL D2+

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.760 V	46.7	Timing 105	296.694 MHz	74.842 k	69.399 k	3.244 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL

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7-2: VL D2-

Test ID 7-2

The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

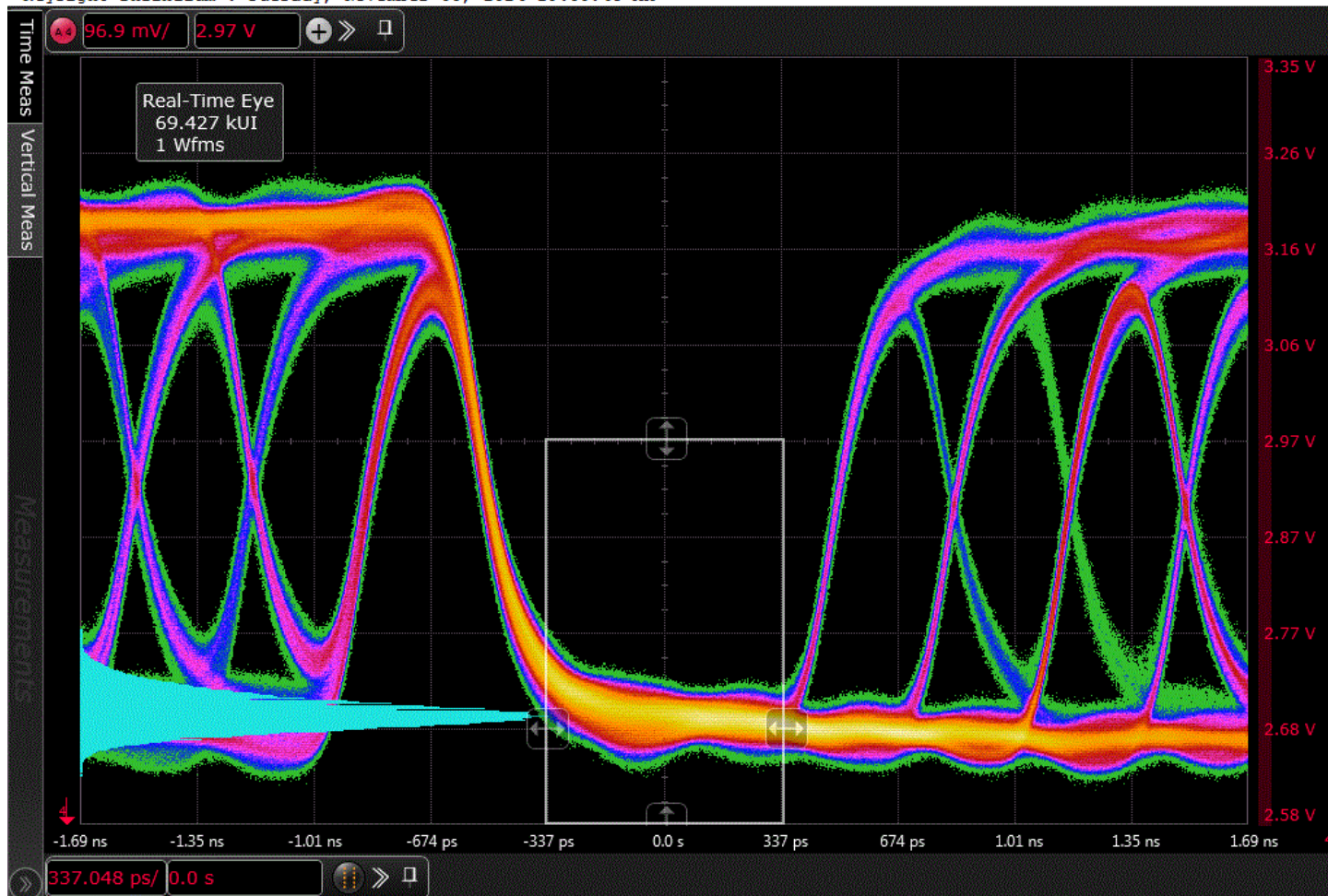
Actual Value Measurement Name: 7-2 VL D2-

Pass Limits: LowerLimit V <= VALUE <= 2.900 V

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	# Edges,VL	# Edges,VH	VH	VL
2.745 V	48.3	Timing 105	296.694 MHz	69.427 k	72.170 k	3.221 V	(See image)

DUT supports clock rates > 165MHz	PassLimit Min (LowerLimit)
true	2.600 V

VL



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7-7: Intra-Pair Skew - Data Lane 2

Test ID 7-7

Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-7 Intra-Pair Skew - D2 Lane

Pass Limits: -150 mTbit <= VALUE <= 150 mTbit

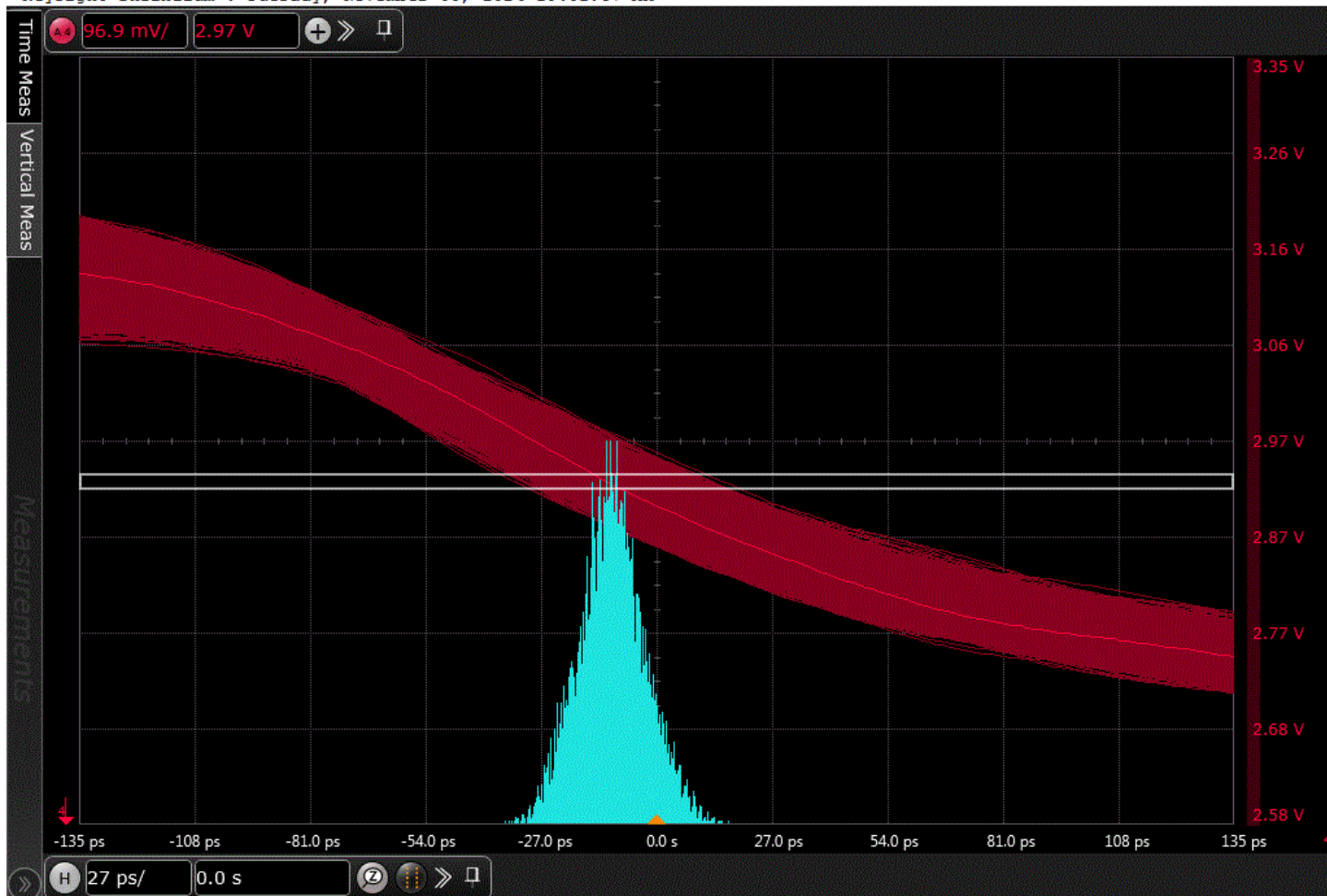
Actual Value	Margin	HDMIAutomationConfig	Max skew (ps)	Min skew (ps)	Mean skew (ps)	Std Dev (ps)	D+ threshold (V)
-34 mTbit	38.7	Timing 105	16.880	-35.230	-10.202	7.664	2.959

D- threshold (V)	Acquisition Bandwidth (GHz)	NumEdges	Test Frequency(MHz)	Data Intra-Pair Skew(ps)
2.927	13.000	12.237000 k	296.694 MHz	-11.600

Intra-Pair Skew Distribution

(See image)

Intra-Pair Skew Distribution



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7-6: Inter-Pair Skew - D0/D1

Test ID 7-6

Inter-pair skew must not exceed $0.20 \times T_{\text{pixel}}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-6 Inter-Pair Skew - D0/D1

Pass Limits: $-200 \text{ mTpixel} \leq \text{VALUE} \leq 200 \text{ mTpixel}$

Actual Value	Margin	HDMI Automation Config	Test Frequency (MHz)	Data Lane A	Data Lane B	Data - Data Inter-Pair Skew (ps)
21 mTpixel	44.8	Timing 105	296.694 MHz	D0	D1	69.471

Triggered Pattern
(no value)

7-6 Inter-Pair Skew - D0/D1



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7-6: Inter-Pair Skew - D0/D2

Test ID 7-6

Inter-pair skew must not exceed $0.20 \times T_{\text{pixel}}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

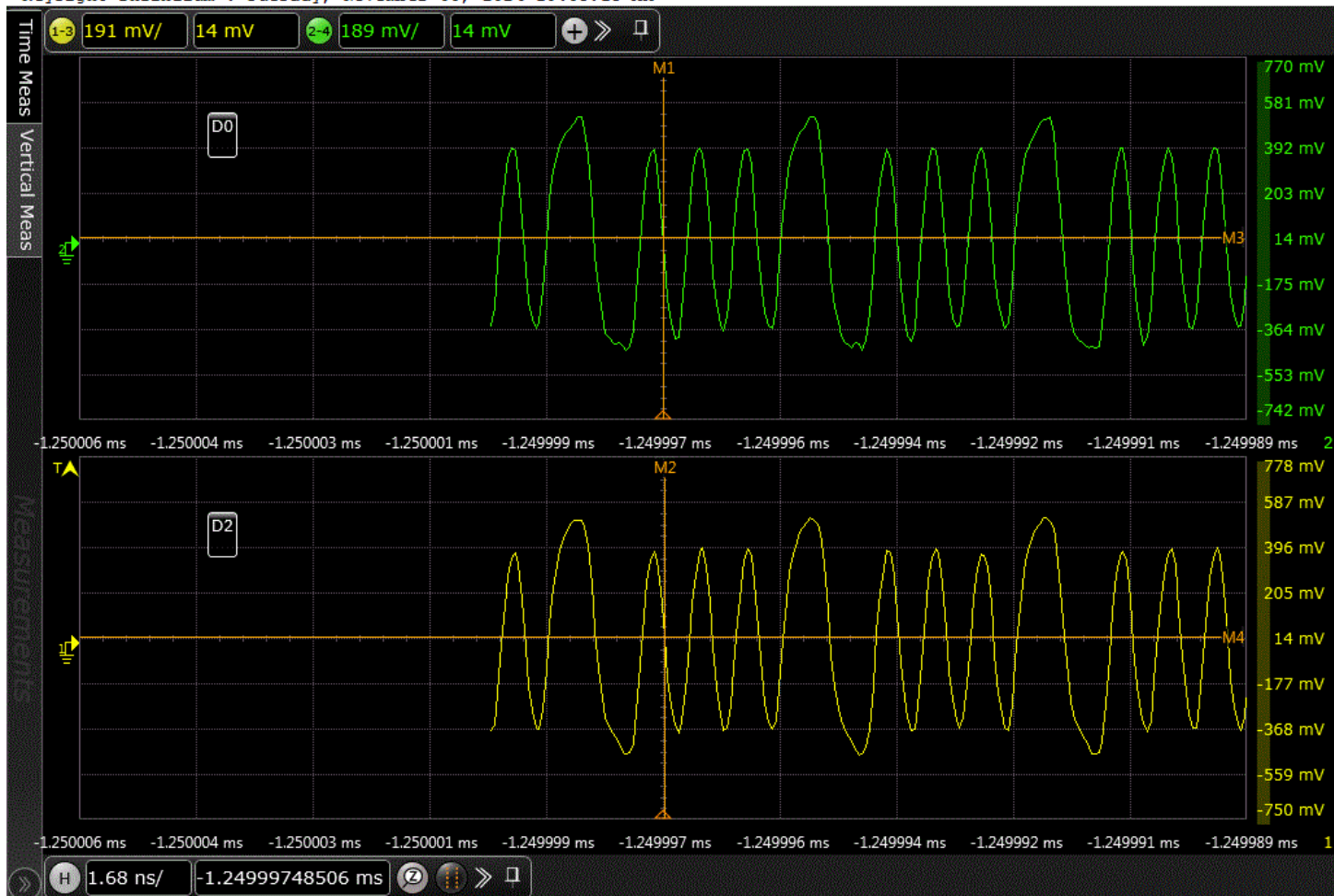
Actual Value Measurement Name: 7-6 Inter-Pair Skew - D0/D2

Pass Limits: $-200 \text{ mTpixel} \leq \text{VALUE} \leq 200 \text{ mTpixel}$

Actual Value	Margin	HDMIAutomationConfig	Test Frequency(MHz)	Data Lane A	Data Lane B	Data - Data Inter-Pair Skew(ps)
-7 mTpixel	48.3	Timing 105	296.694 MHz	D0	D2	-24.587

Triggered Pattern
(no value)

7-6 Inter-Pair Skew - D0/D2

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7-6: Inter-Pair Skew - D1/D2

Test ID 7-6

Inter-pair skew must not exceed $0.20 \cdot T_{\text{pixel}}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Actual Value Measurement Name: 7-6 Inter-Pair Skew - D1/D2

Pass Limits: $-200 \text{ mTpixel} \leq \text{VALUE} \leq 200 \text{ mTpixel}$

Actual Value	Margin	HDMI Automation Config	Test Frequency (MHz)	Data Lane A	Data Lane B	Data - Data Inter-Pair Skew (ps)
-28 mTpixel	43.0	Timing 105	296.694 MHz	D1	D2	-94.904

Triggered Pattern

(no value)

7-6 Inter-Pair Skew - D1/D2

