Power Button. Used to initiate a system power-on and to enter/exit SC7. 3.3V to 1.8V level shifter on the module.

POWER_BTN_N: Open Drain, 3.3V

full system reset (including PMIC)(i.e. From RESET button). 1kΩ pull-up to 1.8V is present on the module.

SYS_RESET_N: Open Drain, 1.8V

System Reset: Connected to NRST_IO of PMIC. Bidirectional reset driven from PMIC to carrier board

from FPGA to FPGA and HDMI from FPGA
千兆网信号，
等长控制在100mil内；
差分阻抗抗100欧。

RX电阻靠近PHY放置
TX电阻靠近FPGA放置

接口走线
内
50mil

电阻靠近
电阻靠近

差分阻抗控等长，
等长控制在100mil内；
差分阻抗控100欧。

近

电容靠近PHY芯片放
support lane flip and polarity correction

automatic P/N correction
FW provision on lane flip

万兆MDI x4高速串行信号，每一条通道速率2.5bps设计，x4组内等长控制10mil，差分阻抗控制100欧。